

Scala2-R

CPU : Sandy Bridge PGA
Chip Set : Intel Cougar Point
GFX : N12P-GV/N12M-GE
Remarks : Huron River Platform

Model Name : Scala2-R
PBA Name : MAIN
PCB Code : BA41-01609A (GCE)
BA41-01608A (NY)
BA41-01610A (HAN)
BA41-01XXXA (GBM)
Dev. Step : ADV
Revision : 0.1
T.R. Date : 2011.01.20

Design	CHECK	APPROVAL
<i>GU HUI</i>	<i>SJ WU</i>	<i>BC LEE</i>

■ Owner : SRDC PD3

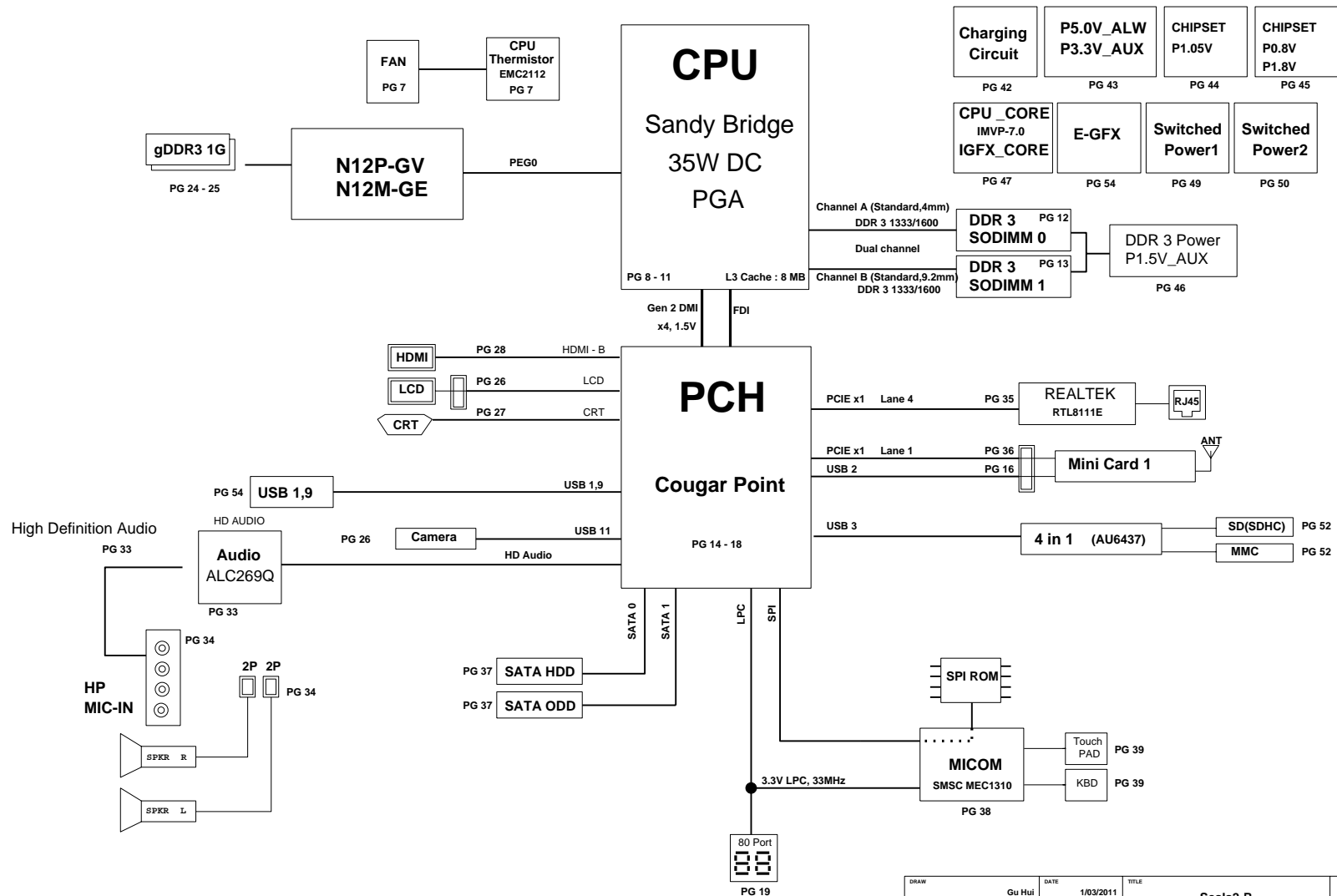
Signature : GUHUI

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sheet06 : Thermal Sensor
sheet07 : CPU
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sheet44 : Power - Switched Power 2
sheet45 : Power - Power Discharge
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sheet47 : Touchpad & LED
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DRAW	Gu Hui	DATE	1/03/2011	Scala2-R MAIN COVER		SAMSUNG ELECTRONICS	
CHECK	SJ Wu	DEV. STEP	ADV				
APPROVAL	BC LEE	REV	rev. 0.1			PART NO.	BA41-01XXXX
MODULE CODE	LAST EDIT		January 20, 2011 18:59:20 PM			PAGE	1 OF 48

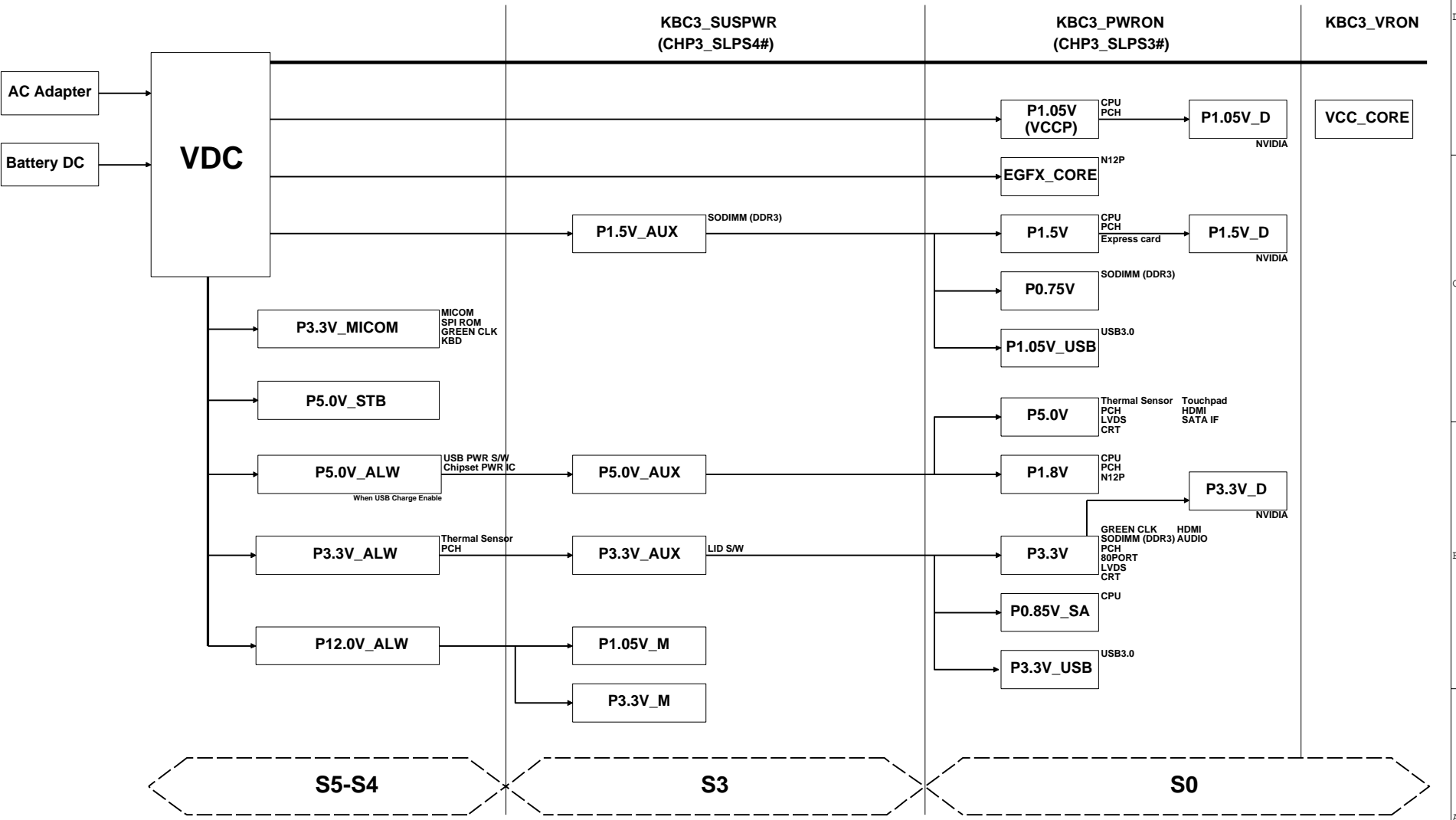
BLOCK DIAGRAM



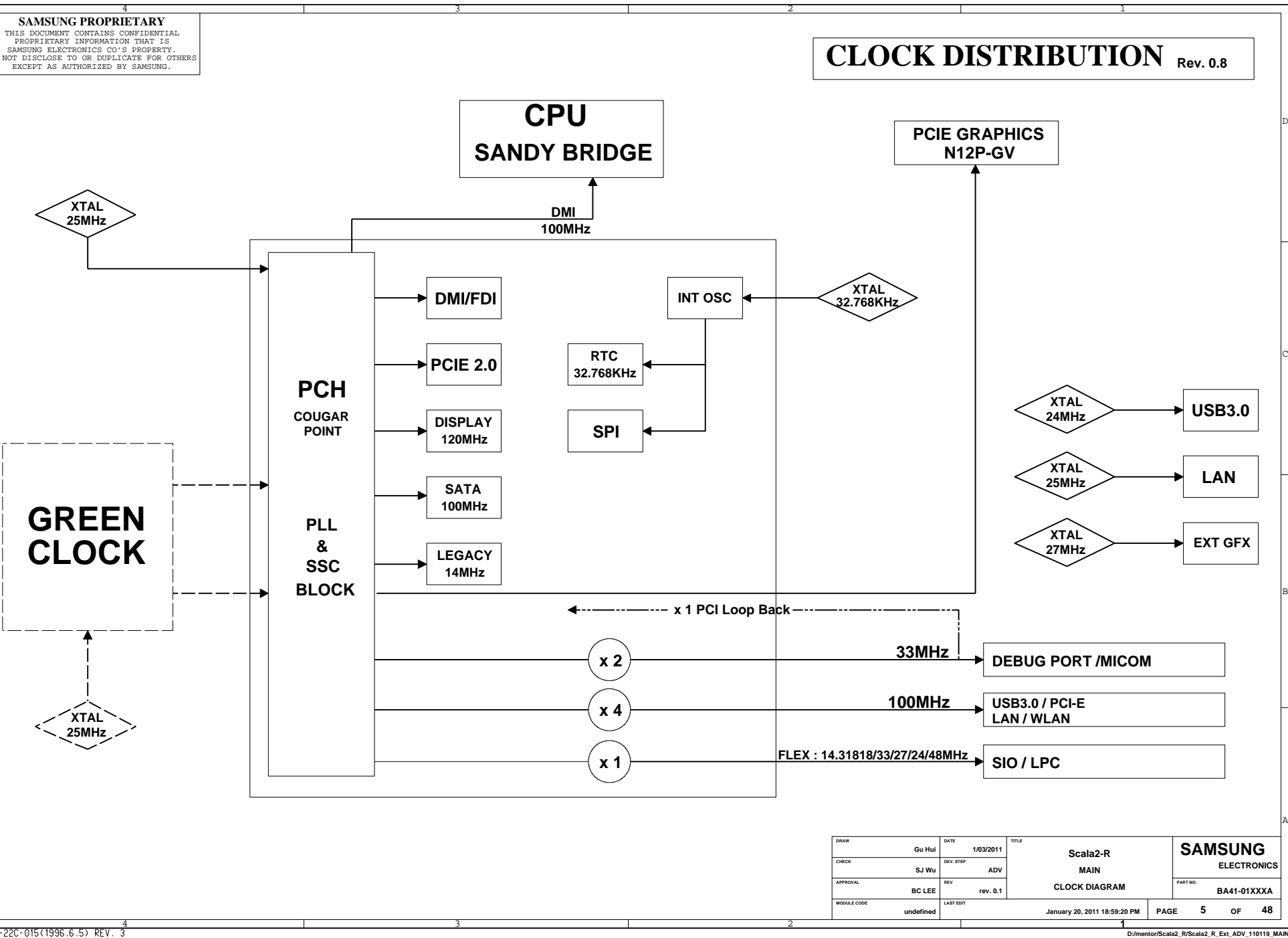
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CHECK	SJ Wu	DEV. STEP	ADV	MAIN		
APPROVAL	BC LEE	REV	rev. 0.1	BLOCK DIAGRAM	PART NO.	
MODULE CODE	undefined	LAST EDIT	January 20, 2011 18:59:20 PM	PAGE	2 OF 48	

POWER DIAGRAM

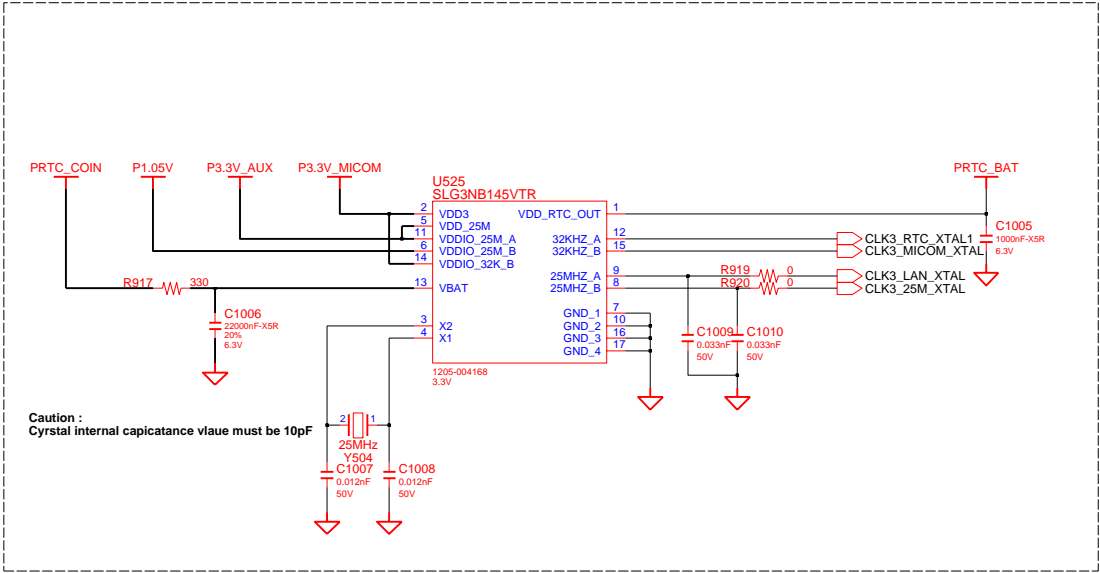
Rev 0.8



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CHECK	SJ Wu	DEV. STEP	ADV	MAIN	POWER DIAGRAM	ELECTRONICS
APPROVAL	BC LEE	REV	rev. 0.1			PART NO.
MODULE CODE	undefined	LAST EDIT	January 20, 2011 18:59:20 PM			BA41-01XXXA
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CLOCK DISTIBUTOR



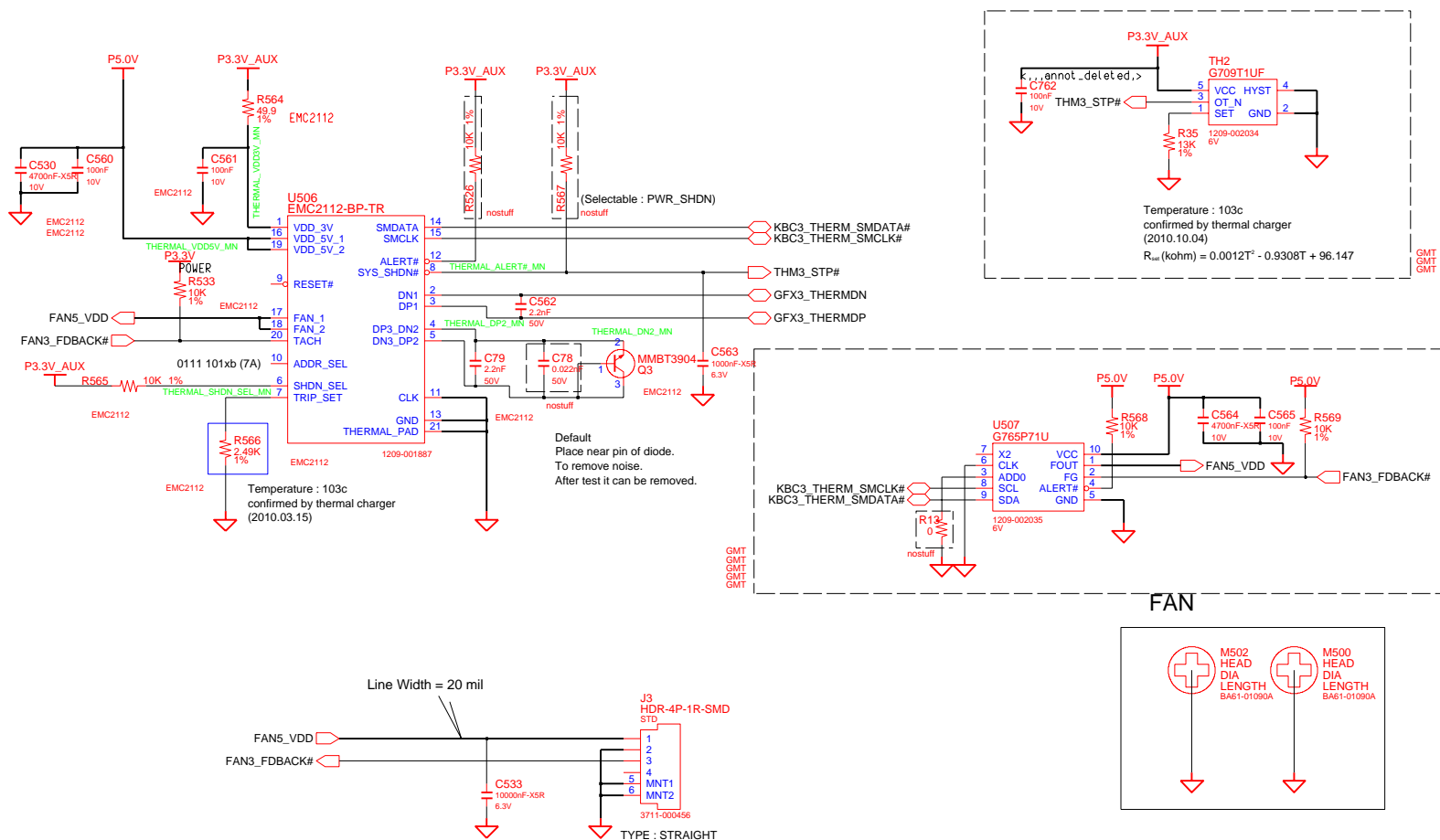
GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK

ENGINEER	DATE	TITLE	SAMSUNG ELECTRONICS PART NO. BA41-XXXXXX
DESIGNED BY	short_date	SCALAZ-R_PV_MAIN	
CHANGED BY	DEV. STEP	Module Name	
FIG. CHK	REV	1.0	
LAST EDIT		last_edit	PAGE 6 OF XX

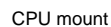
THERMAL SENSOR & FAN CONTROL

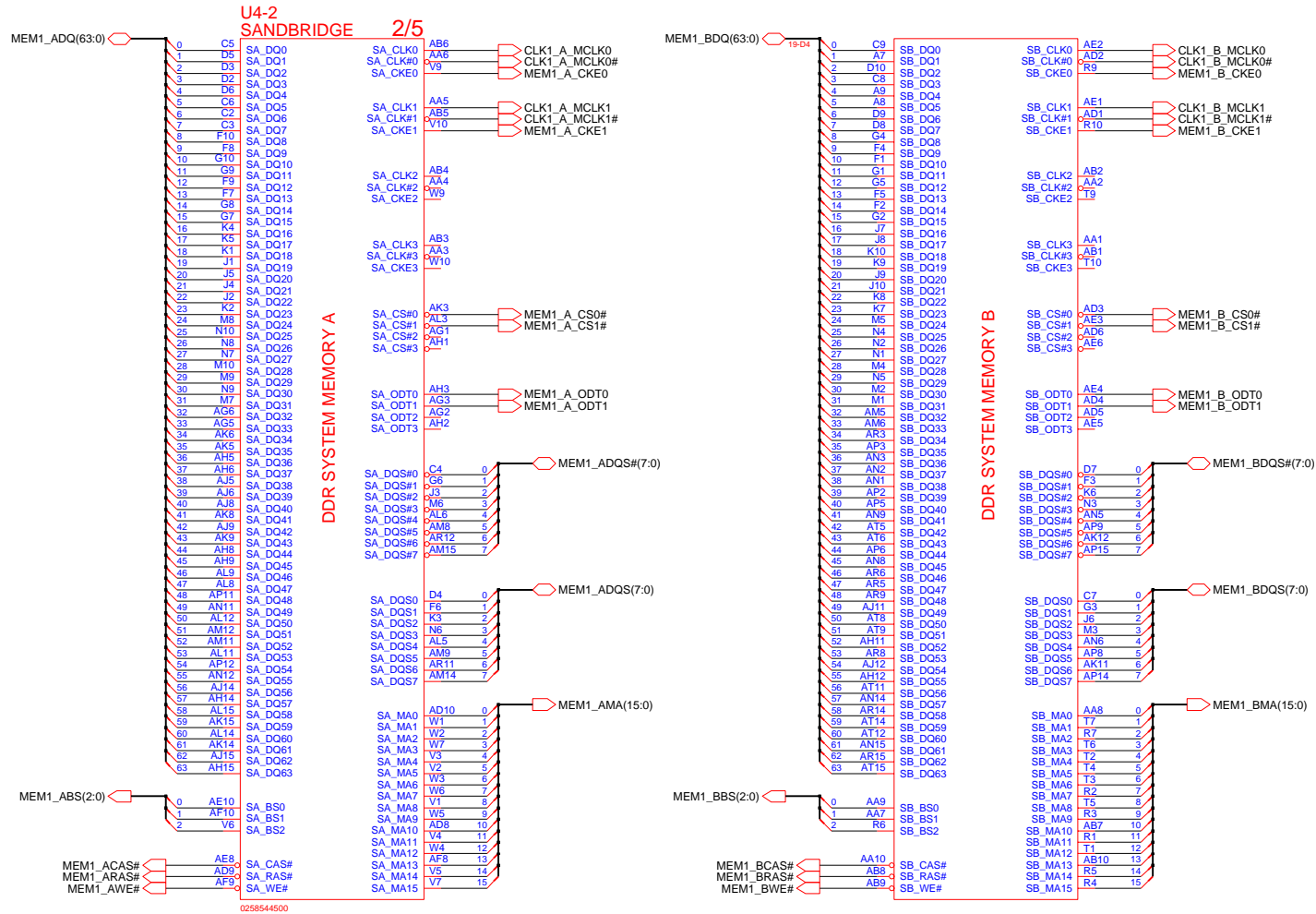
ADDRESSSEL_MODE	
0	0101 111xb
✓ HIGH Z	0111 101xb (7A)
1	0101 110xb

SHDNSEL_MODE	
0	INTEL TR MODE
HIGH Z	AMD CPU/DIODE MODE
✓ 1	EXT.DIODE 2 MODE



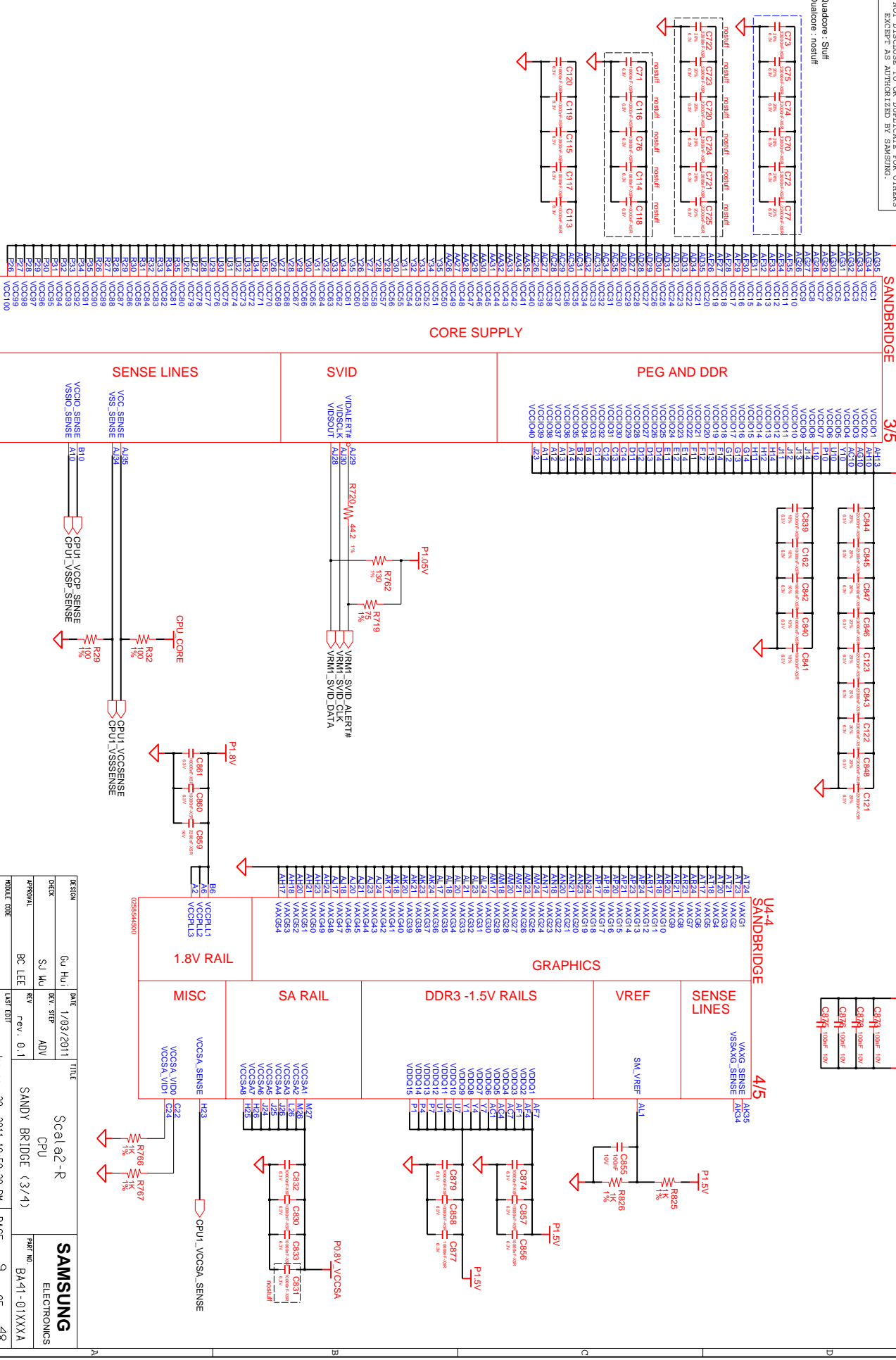
P1.05V

D:/mentor/Scala2_R/Scala2_R_Ext_ADV_110119_MAIN

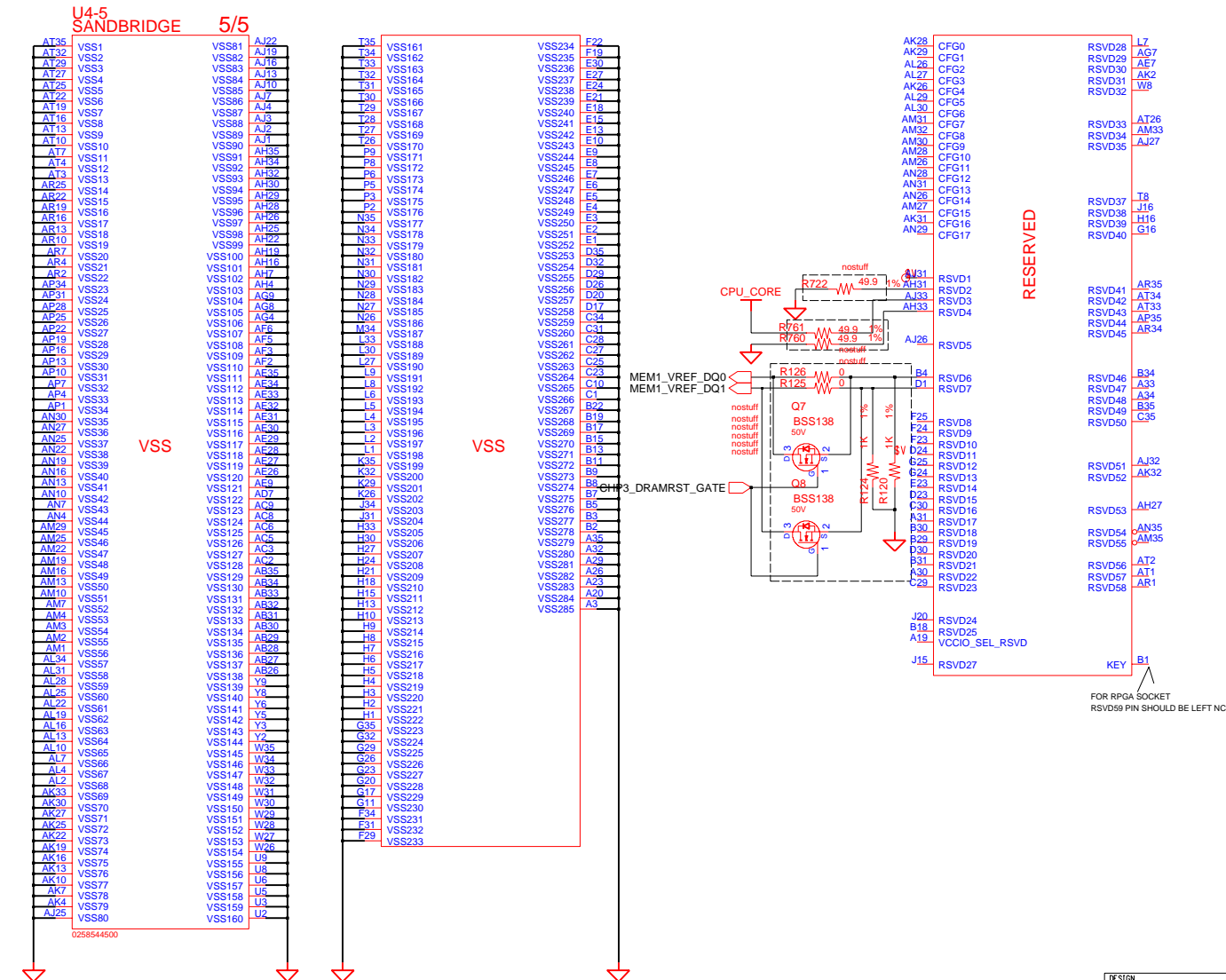


DRAW	Gu Hui	DATE	1/03/2011	TITLE	Scala2-R	SAMSUNG ELECTRONICS
CHECK	SJ Wu	DEV. STEP	ADV	CPU		
APPROVAL	BC LEE	REV	rev. 0.1	SANDY BRIDGE (2/4)	PART NO.	
MODULE CODE	undefined	LAST EDIT	January 20, 2011 18:59:20 PM	PAGE	8 OF 48	

CPU CORE U4-3
SANDBRIDGE



DESIGN	Gu Hu1	DATE	1/03/2011	TITLE	Scal a2-R	SAMSUNG ELECTRONICS
CHECK	SJ MU	REV. STEP	ADV	CPU		
APPROVAL	BC LEE	REV	rev. 0.1	SANDY BRIDGE (3/4)	PART NO. BA41-01XXXXA	
MODULE CODE		LAST EDIT	January 20, 2011 18:59:20 PM	PAGE	9 OF 48	



CFG Straps for Processor

PEG STATIC LANE REVERSAL - CFG2 IS FOR THE 16X	
CFG2	1 : (DEFAULT) NORMAL OPERATION 0 : LANE REVERSED

PCIe PORT BIFURCACTION STRAPS	
CFG[6:5]	11 : (DEFAULT) X16 - DEVICE 1 FUNCTIONS 1 AND 2 DISABLED 10 : X8, X8 - DEVICE 1 FUNCTION 1 ENABLED ; FUNCTION 2 DISABLED 01 : RESERVED - (DEVICE 1 FUNCTION 1 DISABLED ; FUNCTION 2 ENABLED) 00 : X8, X4, X4 - DEVICE 1 FUNCTIONS 1 AND 2 ENABLED

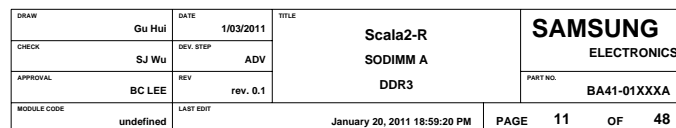
Display Port Presence	
CFG4	1 : Disabled - No DP device is connected to eDP 0 : Enabled - (DP device is connected to eDP)

PEG DEFER TRAINING	
CFG7	1 : (DEFAULT) PEG TRAIN IMMEDIATELY FOLLOWING XCRESETB DEASSERTION 0 : PEG WAIT FOR BIOS FOR TRAINING

DESIGN	Gu Hui	DATE	1/03/2011	TITLE	Scala2-R CPU	SAMSUNG ELECTRONICS
CHECK	SJ Wu	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	rev. 0.1		SANDY BRIDGE (4/4)	PART NO. BA41-01XXXXA
MODULE CODE		LAST EDIT	January 20, 2011 18:59:20 PM	PAGE	10	OF 48

DDR SO-DIMM #0

P/N : 3709-001656 (Foxconn)



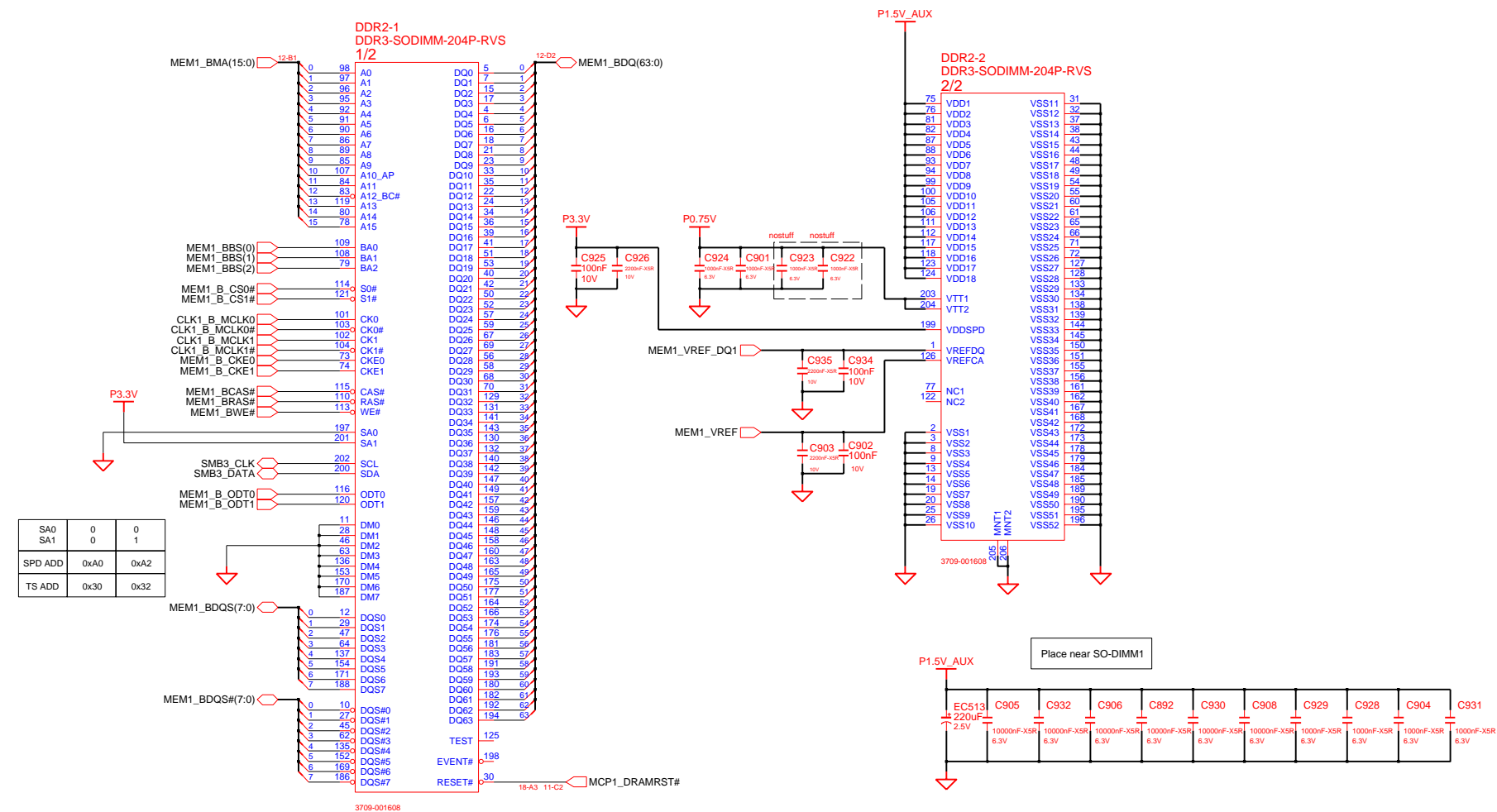
SO-DIMM#1 : 1st SO-DIMM

DDR SO-DIMM #1

Height : 4 mm (REVERSE)

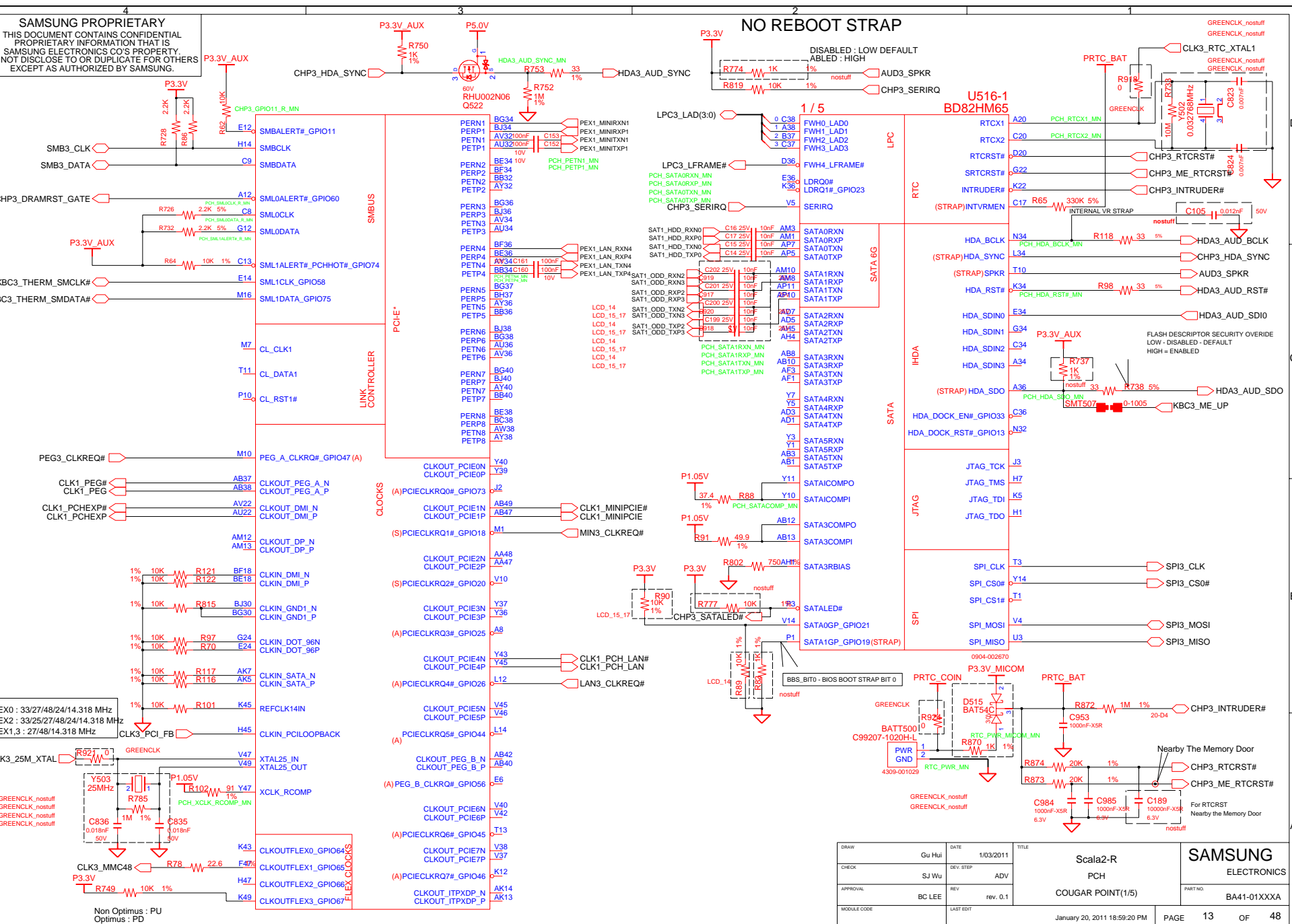
P/N : 3709-001608 (CONCRAFT)

P/N : 3709-001654 (Foxconn)

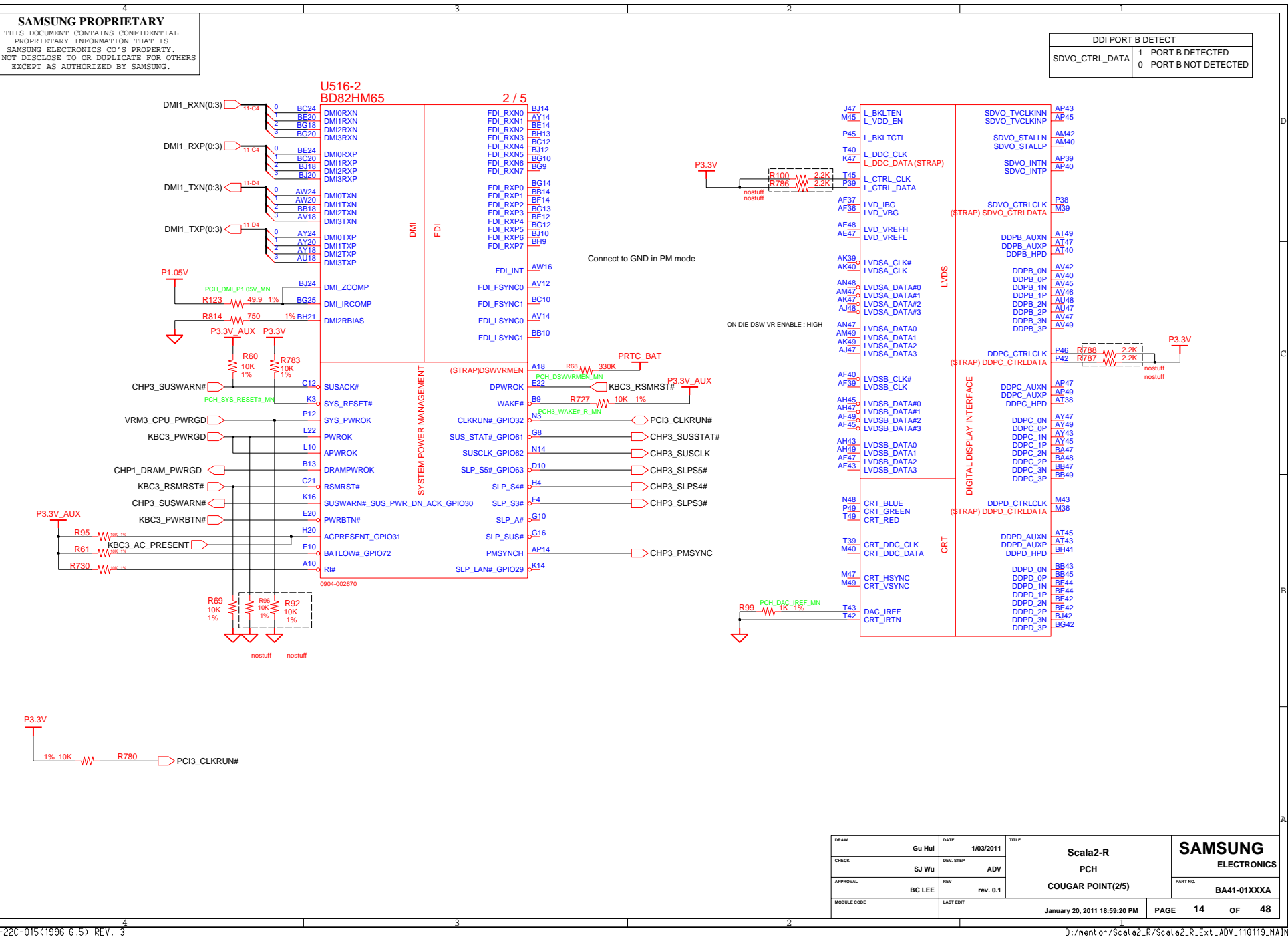


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CHECK	SJ Wu	DEV. STEP	ADV		SODIMM B	ELECTRONICS
APPROVAL	BC LEE	REV	REV. 0.1		DDR3	PART NO.
MODULE CODE		LAST EDIT				BA41-01XXXA
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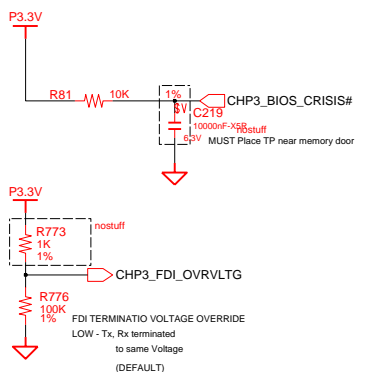
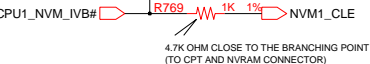
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CHECK	SJ WU	DEV. STEP	ADV		
APPROVAL	BC LEE	REV	rev. 0.1		
MODULE CODE	LAST EDIT				
				January 20, 2011 18:59:20 PM	PAGE 13 OF 48



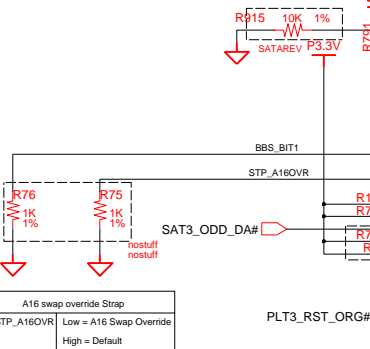
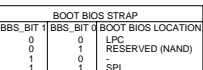
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CPU1_NVM_IVB#  R769 1K 1% NVM1_CLE

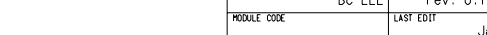
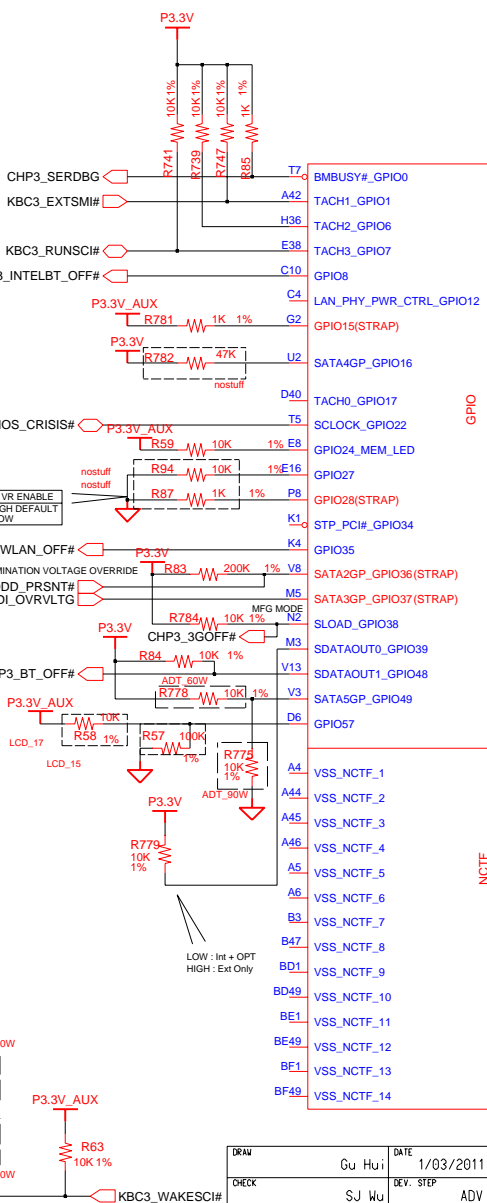
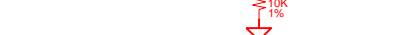
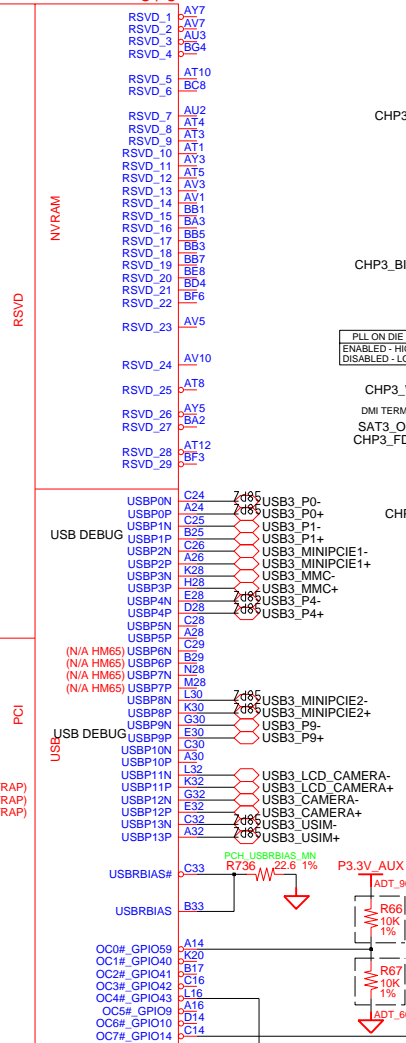
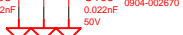
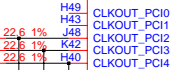
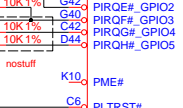
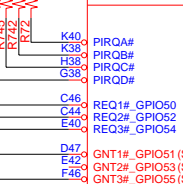
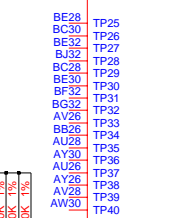
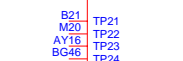
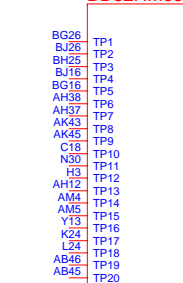
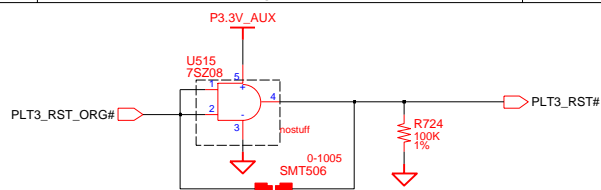
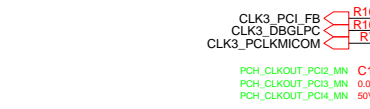
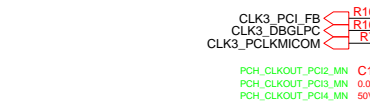
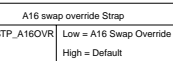
4.7K OHM CLOSE TO THE BRANCHING POINT
(TO CPT AND NVRAM CONNECTOR)



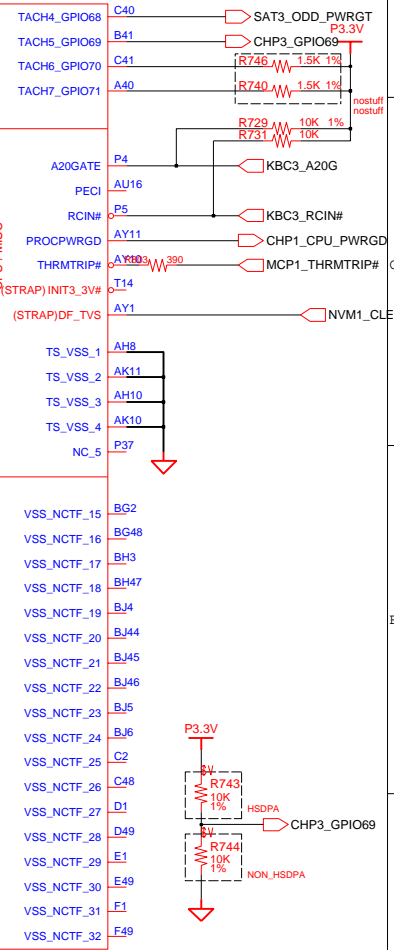
BOOT BIOS STRAP		
BBS_BIT 1	BBS_BIT 0	BOOT BIOS LOCATION
0	0	LPC
0	1	RESERVED (NAND)
1	0	-
1	1	SPI



A16 swap override Strap	
TP_A16OVR	Low = A16 Swap Override High = Default

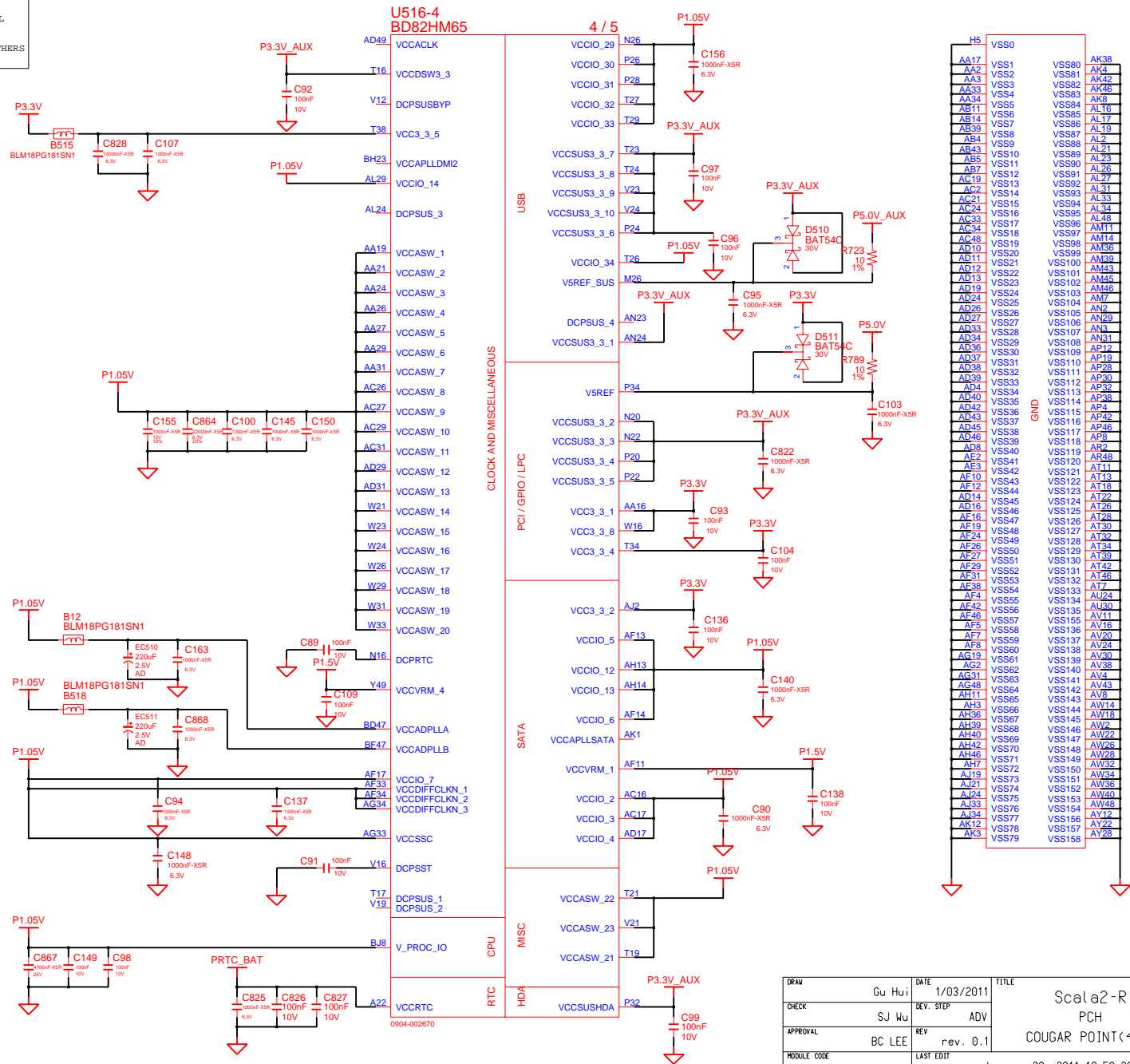


	PU	PD
GPIO 39	EXT ONLY	INT + OPT
GPIO 69	HSDPA	NON HSDPA
GPIO 70		
GPIO 71		
GPIO 57		



DRAW		Gu Hui	DATE	1/03/2011	TITLE		SAMSUNG ELECTRONICS	
#	CHECK	SJ Wu	REV. STEP	ADV				
	APPROVAL	BC LEE	REV	rev. 0.1	COUGAR POINT(3/5)	PART NO.	BA41-01XXXXA	
MODULE CODE			LAST EDIT		January 20, 2011 18:59:20 PM		PAGE	15 OF 48

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CHECK	SJ Wu	DEV. STEP	ADV		PCH	
APPROVAL	BC LEE	REV	rev. 0.1		COUGAR POINT(4/5)	PART NO. BA41-01XXXXA
MODULE CODE		LAST EDIT			January 20, 2011 18:59:20 PM	
					PAGE 16 OF 60	

5 / 5

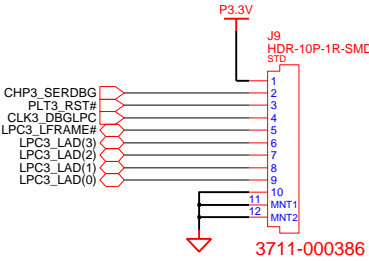
D:/mentor/Scala2 R/Scala2 R Ext ADV 110119 MAIN

3

2

1

80H PORT DEBUG

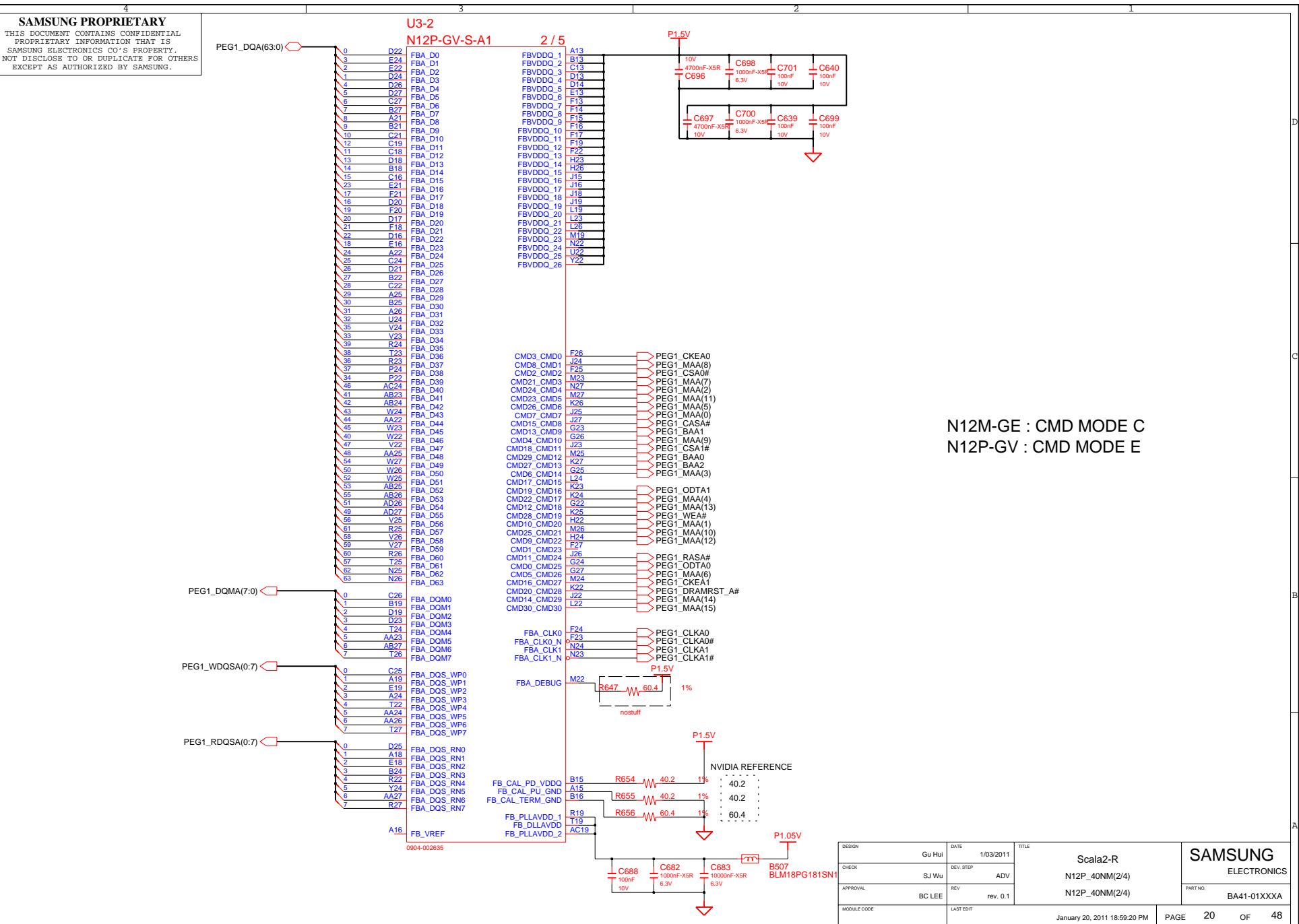


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APPROVAL	BC LEE	REV	rev. 0.1			
MODULE CODE		LAST EDIT	January 20, 2011 18:59:20 PM	PAGE	18	OF 48

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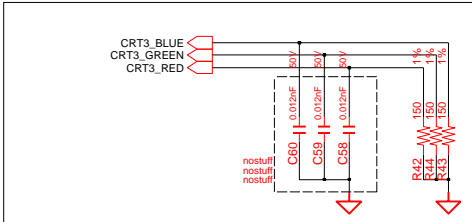


DESIGN	Gu Hui	DATE	1/03/2011	Scala2-R N12P_40NM(1/4) N12P_40NM(1/4)	SAMSUNG ELECTRONICS
CHECK	SJ Wu	DEV. STEP	ADV		
APPROVAL	BC LEE	REV	rev. 0.1		
MODULE CODE	LAST EDIT				
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DESIGN	Gu Hui	DATE	1/03/2011	Scala2-R N12P_40NM(3/4) N12P_40NM(3/4)	SAMSUNG ELECTRONICS	
CHECK	SJ WU	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	rev. 0.1			
				PART NO.	BA41-01XXXX	
MODULE CODE		LAST EDIT			January 20, 2011 18:59:20 PM	PAGE 21 OF 48

The diagram illustrates the GPU interface connections for the GFX3_STRAP0, GFX3_STRAP1, GFX3_ROM_SO, and GFX3_ROM_SI signals. Each signal line is connected to a pull-up resistor (R695, R696, R697, R698) to P3.3V and a pull-down resistor (R692, R693, R694, R695) to GND. The strap configurations are detailed in the table below.

Strap	Configuration	Value
GFX3_STRAP0	User Strap	1111
	EDID is used	1000 - 1100
	Customer defined	0000 - 0001
	1024 x 768	0010
GFX3_STRAP1	GPU PCIe Interface Strap	1110
	N12M-GE	0110
	N12P-GV	0110
	DeskTop	0000
GFX3_ROM_SO	Int PCIe Clock - 277MHz(default)	
	Aperture Size - 256MB(default)	
	I2C Address of GPU - 0x9E(default)	
	Device Type - 3D Device(Optimus)	
GFX3_ROM_SI	Memory Configuration :	
	Samsung 64M x 16 gDDR3	0011
GFX3_ROM_SI	Samsung 128M x 16 gDDR3	0111

Diagram illustrating the connection of the ROMSO and SCLK signals to the N12M-GE board. The ROMSO signal is connected to the N12M-GE pin 0x0A7A (1010 / 1010). The SCLK signal is connected to the N12M-GE pin 1010 / 1010. The diagram shows the ROMSO and SCLK signals connected to the N12M-GE pin 0x0A7A (1010 / 1010). The SCLK signal is connected to the N12M-GE pin 1010 / 1010. The diagram shows the ROMSO and SCLK signals connected to the N12M-GE pin 0x0A7A (1010 / 1010).

GFX3_ROM_SCLK → R682 POWER 1%

GFX3_STRAP2 → R697 4.99K 1%

GFX3_ROM _SCLK	N12P-GV	5K PU
-------------------	---------	-------

GFX3 _STRAP2	N12P-GV	5K PD
-----------------	---------	-------

N12P-GE : 0x10 **50** (1000 / 0000)

GFX3_STRAP3
GFX3_STRAP4

R650 4.90K 1%
R446 10K 1%

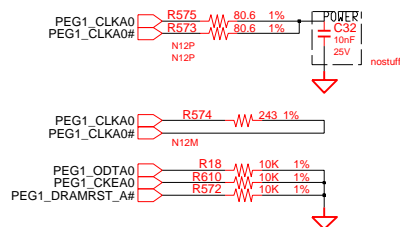
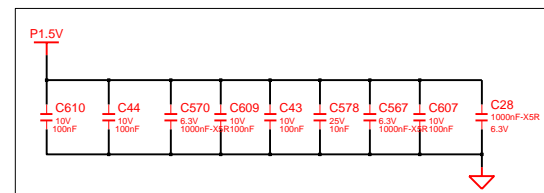
GFX3 _STRAP3	Audio for Digital Display Optimus - 0x0	1000
-----------------	---	-------------

GFX3 _STRAP4	Reserved Reserved PCIe 2.0 support Reserved	0001
-----------------	--	-------------

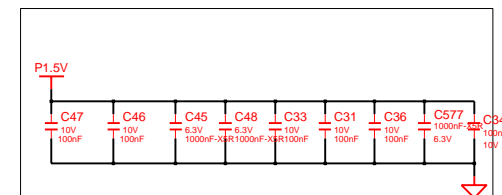
N12P
N12P
N12P

U3-5		N12P-GV-S-A1		C15
B2	GND_1			D15
B5	GND_2	NC_1		
B8	GND_3	NC_2		
B11	GND_4			
B14	GND_5			
B17	GND_6			
B20	GND_7			
B23	GND_8			
B26	GND_9			
E2	GND_10			
E5	GND_11			
E8	GND_12			
E11	GND_13			
E17	GND_14			
E20	GND_15			
E23	GND_16			
E26	GND_17			
H2	GND_19			
H5	GND_20			
J11	GND_21			
J14	GND_22			
J17	GND_23			
K9	GND_24			
K19	GND_25			
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L17	GND_34			
M12	GND_35			
M13	GND_36			
M14	GND_37			
M15	GND_38			
M16	GND_39			
P2	GND_40			
P5	GND_41			
P9	GND_42			
P19	GND_43			
P22	GND_44			
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T12	GND_46			
T13	GND_47			
T14	GND_48			
T15	GND_49			
T16	GND_50			
U2	GND_51			
U5	GND_52			
U11	GND_53			
U12	GND_54			
U13	GND_55			
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U15	GND_57			
U16	GND_58			
U17	GND_59			
U23	GND_60			
U26	GND_61			
Y9	GND_62			
Y19	GND_63			
W11	GND_64			
W14	GND_65			
W17	GND_66			
Y2	GND_67			
Y5	GND_68			
Y23	GND_69			
Y26	GND_70			
AC2	GND_71			
AC5	GND_72			
AC8	GND_73			
AG11	GND_74			
AC14	GND_75			
AC17	GND_76			
AC20	GND_77			
AC23	GND_78			
AC26	GND_79			
AF2	GND_80			
AF5	GND_81			
AF8	GND_82			
AF11	GND_83			
AF14	GND_84			
AF17	GND_85			
AF20	GND_86			
AF23	GND_87			
AF26	GND_88			
	GND_89			

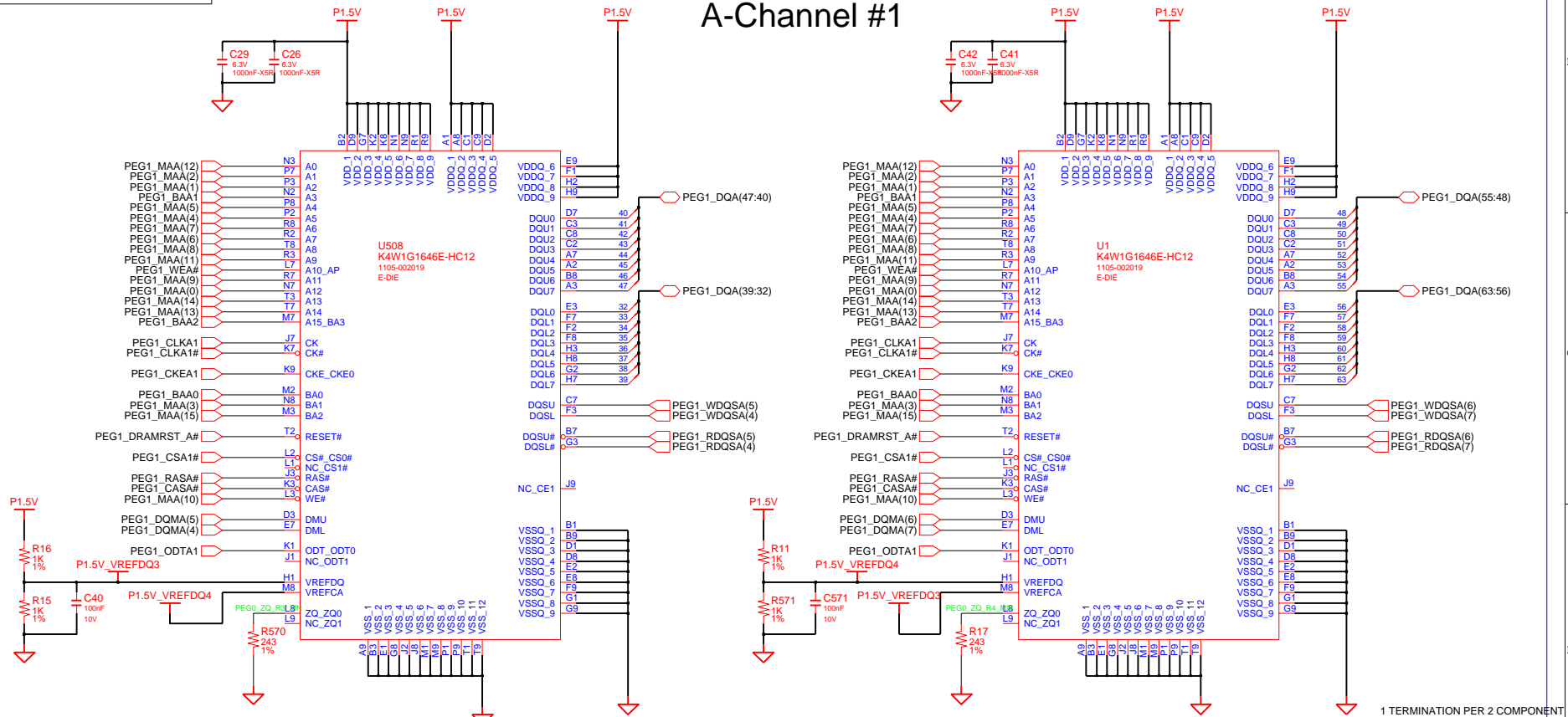
DESIGN	Gu Hui	DATE	1/03/2011	<div>Scala2-R</div> <div>N12M_40NM(4/4)</div> <div>N12P_40NM(4/4)</div>	<div>SAMSUNG</div> <div>ELECTRONICS</div>	
CHECK	SJ WU	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	rev. 0.1		PART NO.	BA41-01XXXX
MODULE CODE	LAST EDIT				January 20, 2011 18:59:20 PM	PAGE 22 OF 48



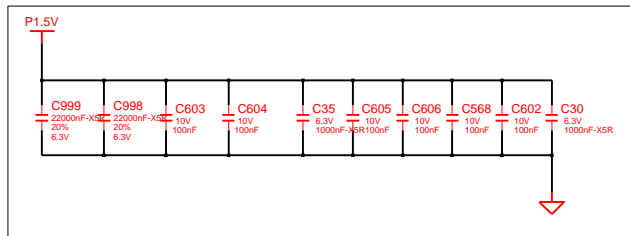
Place near to VDDQ

D:/mentor/Scala2_R/Scala2_R_Ext_ADV_110119_MAIN

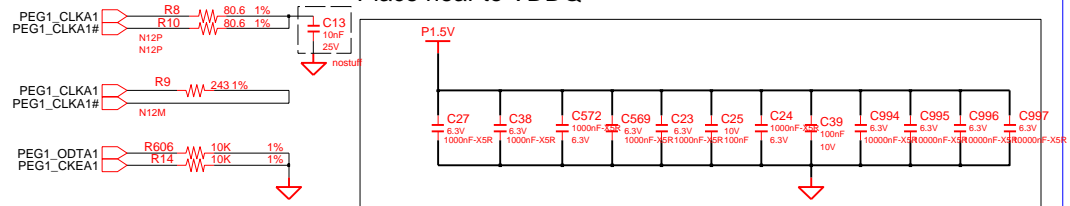
A-Channel #1



Place near to VDDQ



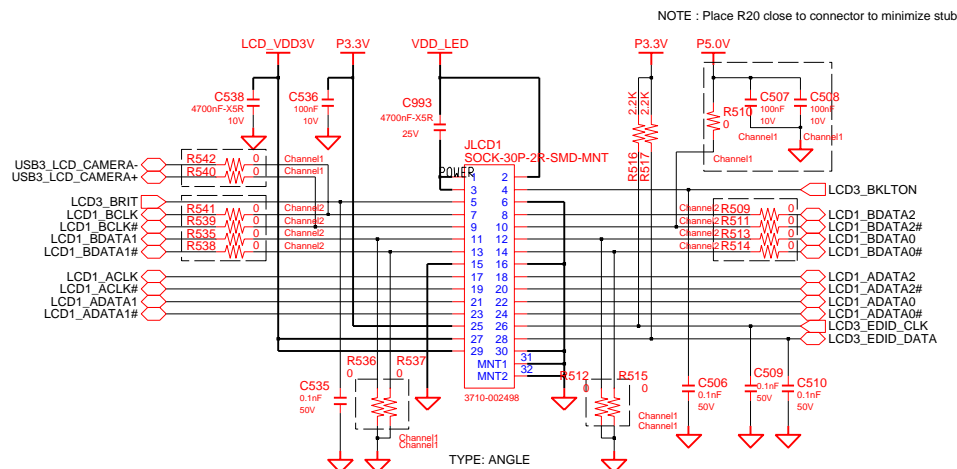
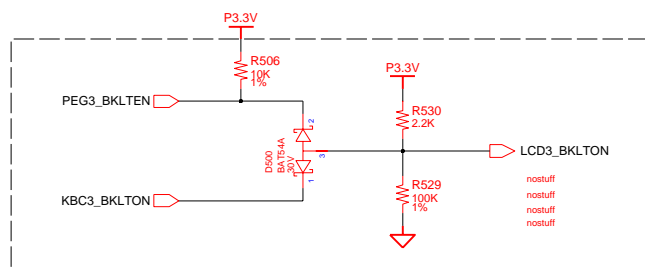
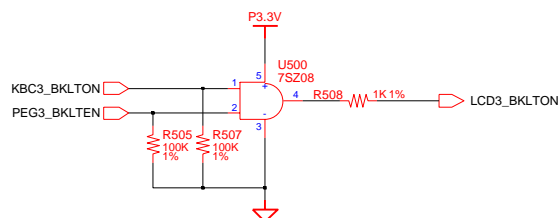
Place near to VDDQ



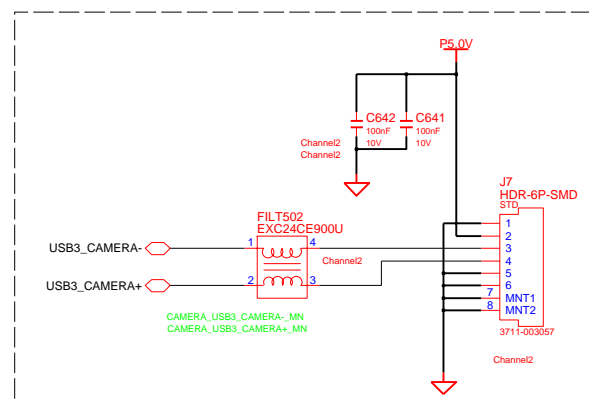
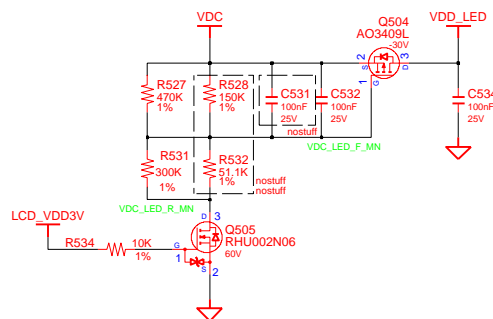
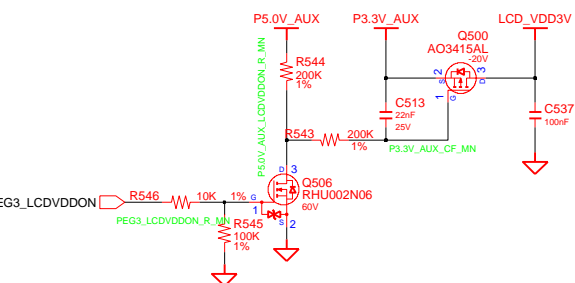
DESIGN	Gu Hui	DATE	1/03/2011	TITLE	Scala2-R	SAMSUNG ELECTRONICS
CHECK	SJ Wu	DEV. STEP	ADV	GRAPHIC_MEM A#1		
APPROVAL	BC LEE	REV	rev. 0.1	GRAPHIC_MEM A#1		
MODULE CODE		LAST EDIT				
				January 20, 2011 18:59:20 PM	PAGE 24 OF 48	PART NO. BA41-01XXA


1Ch. LCD Connector + CAMERA

1Ch. LCD Connector + CAMERA



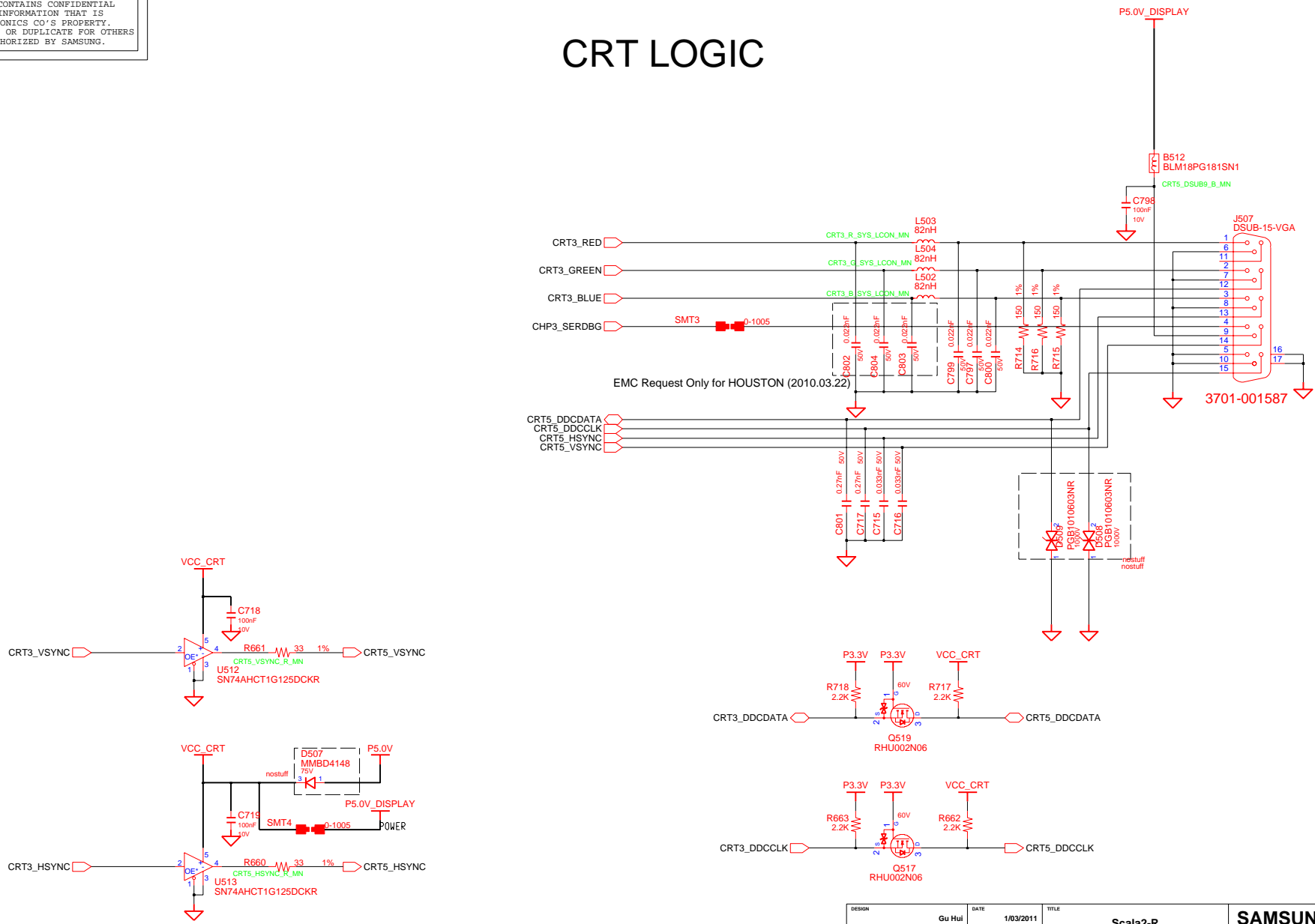
LED Power



DESIGN	Gu Hui	DATE	1/03/2011	Scala2-R GRAPHICS_IF LVDS	
CHECK	SJ Wu	DEV. STEP	ADV		
APPROVAL	BC LEE	REV	rev. 0.1		
MODULE CODE	LAST EDIT		January 20, 2011 18:59:20 PM		

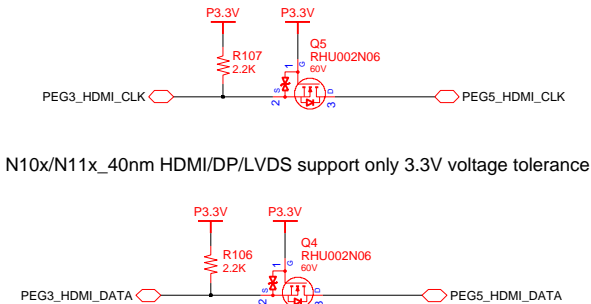
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CRT LOGIC

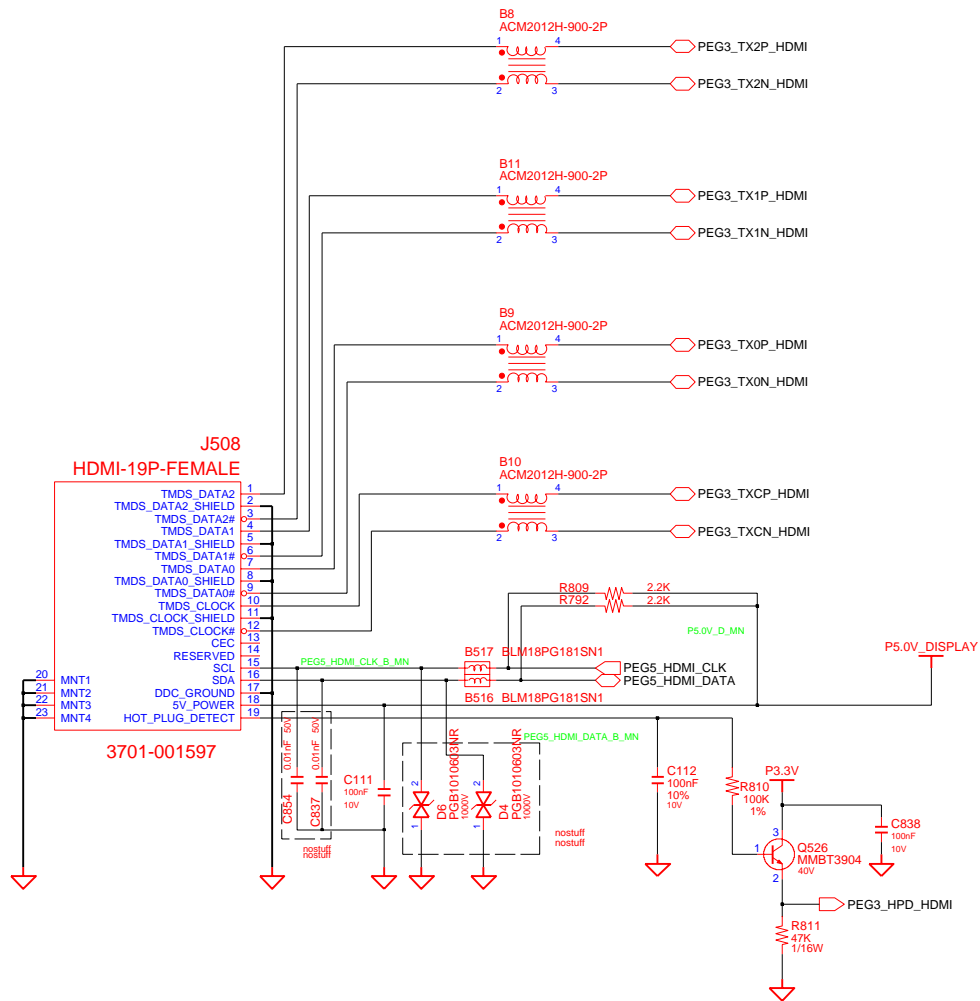


HDMI Graphic

FOR HDMI VERIFICATION TEST

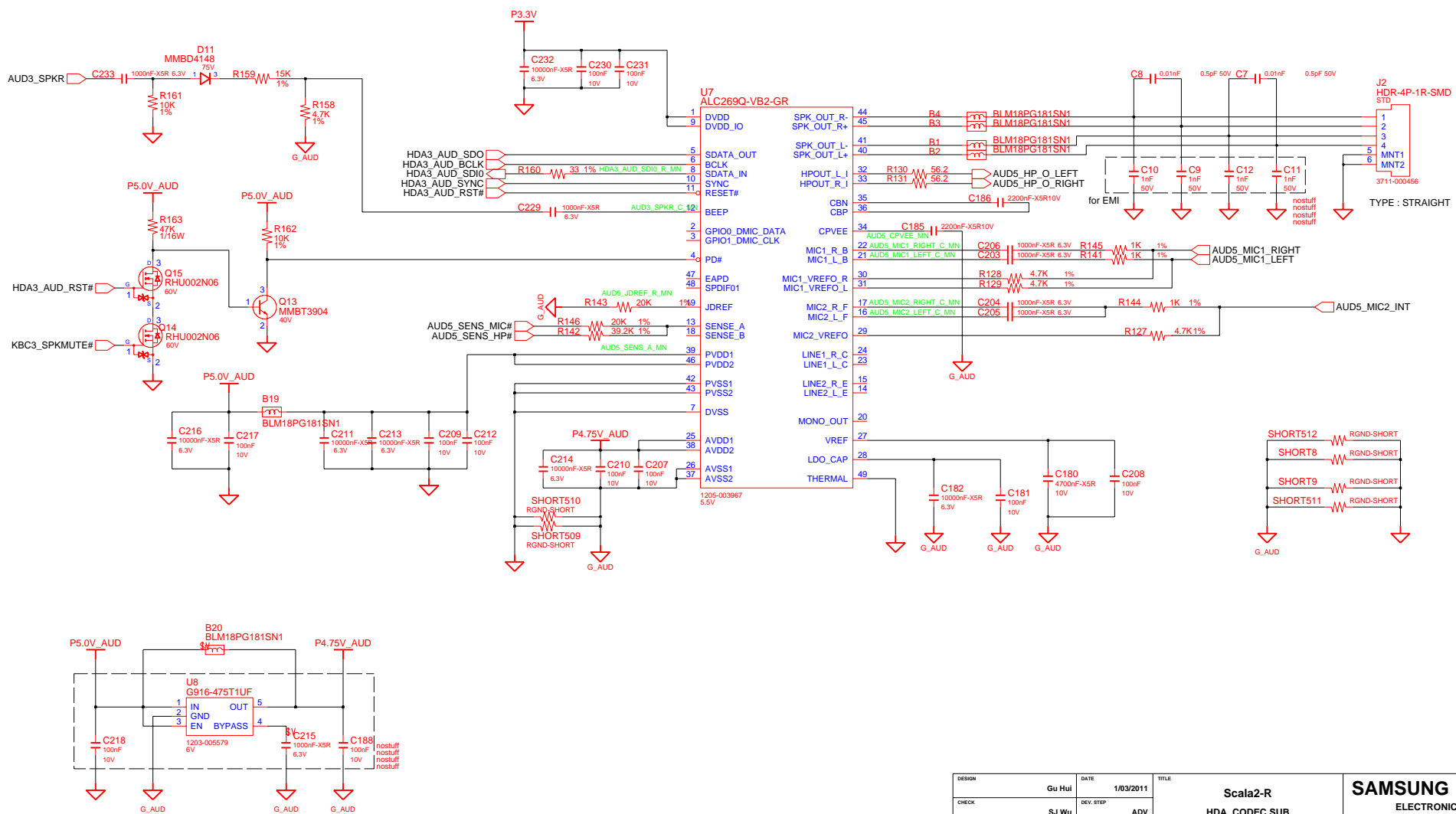


N10x/N11x_40nm HDMI/DP/LVDS support only 3.3V voltage tolerance



DESIGN	Gu Hui	DATE	1/03/2011	Scala2-R GRAPHICS_IF HDMI		SAMSUNG ELECTRONICS			
CHECK	SJ Wu	DEV. STEP	ADV						
APPROVAL	BC LEE	REV	rev. 0.1						
MODULE CODE		LAST EDIT		January 20, 2011 18:59:20 PM		PAGE	27	OF	48

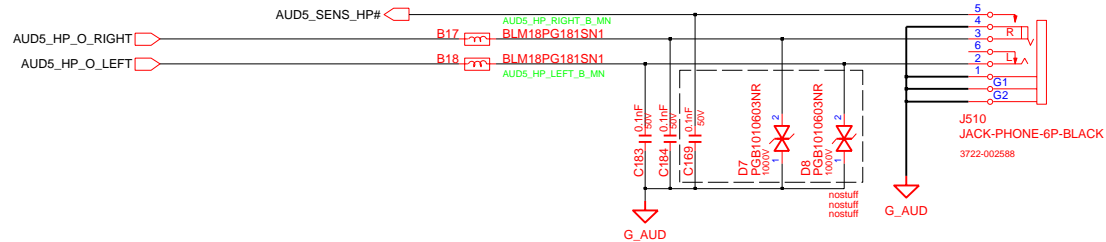
HD AUDIO



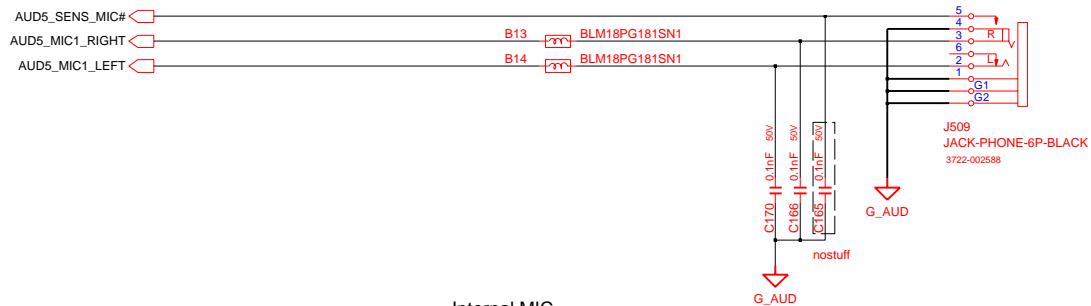
DESIGN	Gu Hui	DATE	1/03/2011	TITLE	Scala2-R
CHECK	SJ Wu	DEV. STEP	ADV	HDA_CODEC SUB	
APPROVAL	BC LEE	REV	rev. 0.1	AUDIO CODEC ALC269 SUB	
MODULE CODE		LAST EDIT			
				January 20, 2011 18:59:20 PM	PAGE 28 OF 48

SAMSUNG
ELECTRONICS
PART NO.
BA41-01XXXXA

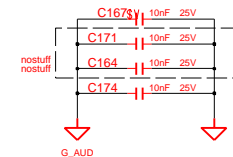
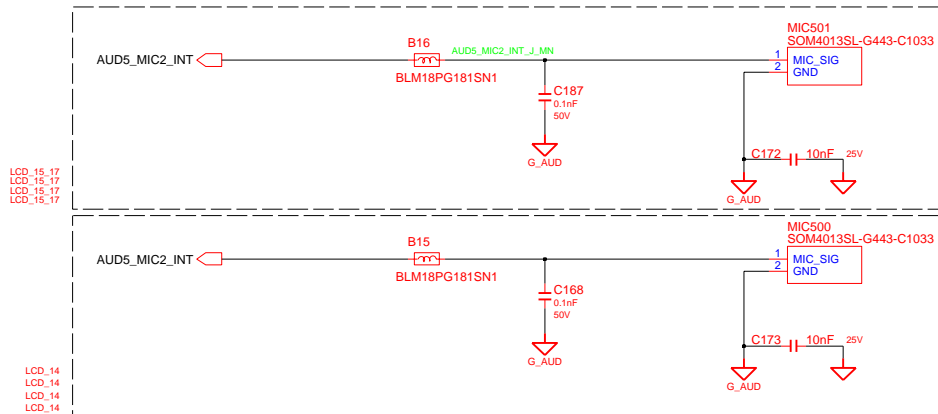
HEADPHONE



MIC JACK

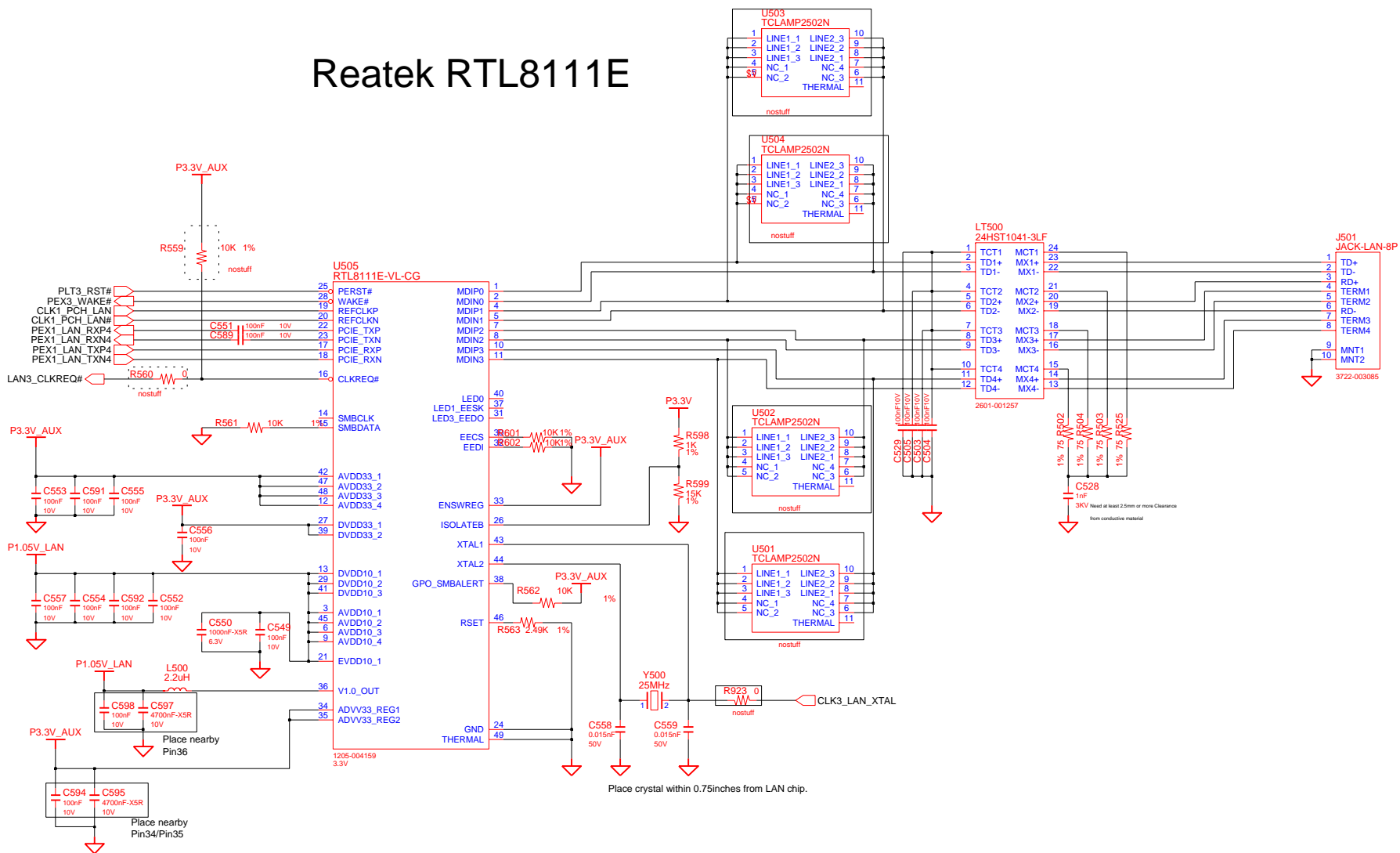


Internal MIC



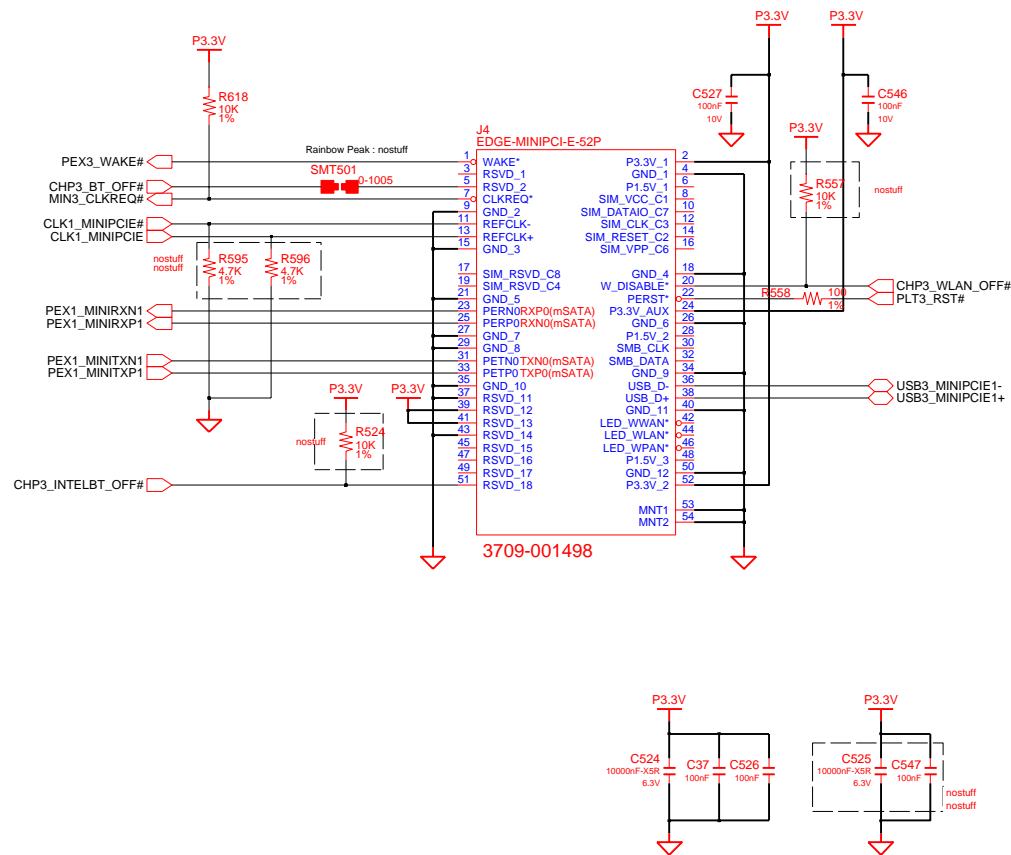
DESIGN	Gu Hui	DATE	1/03/2011	Scala2-R HDA_CODEC & LED SUB AUDIO JACK & LED SUB	SAMSUNG ELECTRONICS PART NO. BA41-01XXXX
CHECK	SJ WU	DEV. STEP	ADV		
APPROVAL	BC LEE	REV	rev. 0.1		
MODULE CODE		LAST EDIT	January 20, 2011 18:59:20 PM		
				PAGE	29 OF 48

Reatek RTL8111E



DESIGN	Gu Hui	DATE	1/03/2011	Scala2-R LAN LAN_Realtek_RTL8111	SAMSUNG ELECTRONICS
CHECK	SJ Wu	DEV_STEP	ADV		
APPROVAL	BC LEE	REV	rev. 0.1		
MODULE CODE	LAST EDIT				
				January 20, 2011 18:59:20 PM	PAGE 30 OF 48

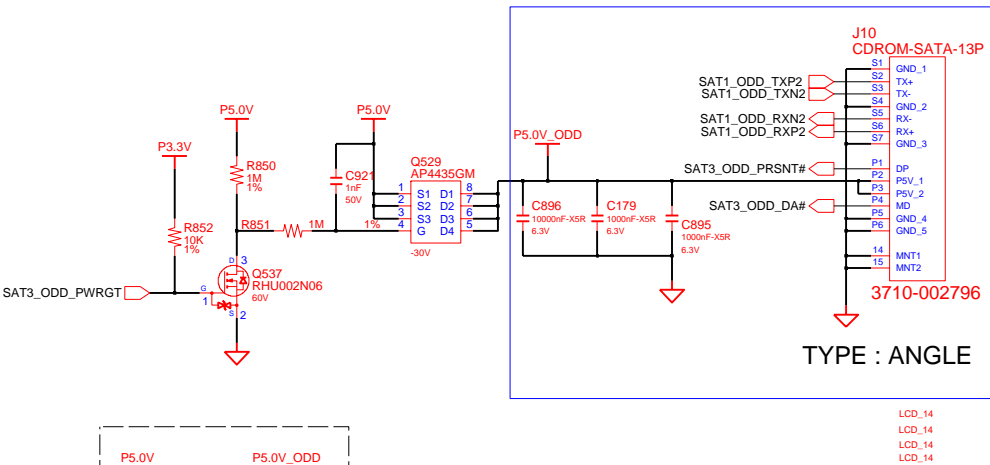
WLAN, 4mm



DESIGN	Gu Hui	DATE	1/03/2011	TITLE	Scala2-R	SAMSUNG ELECTRONICS
CHECK	SJ Wu	DEV. STEP	ADV	MINI_PCIE_CONN		
APPROVAL	BC LEE	REV	rev. 0.1	WLAN		
MODULE CODE		LAST EDIT		January 20, 2011 18:59:20 PM	PAGE 31 OF 48	PART NO. BA41-01XXXA

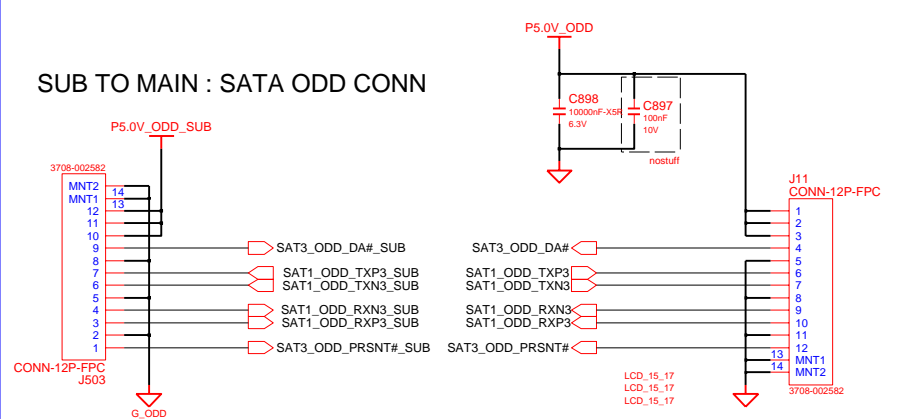
SATA I/F CONN

SATA ODD CONN

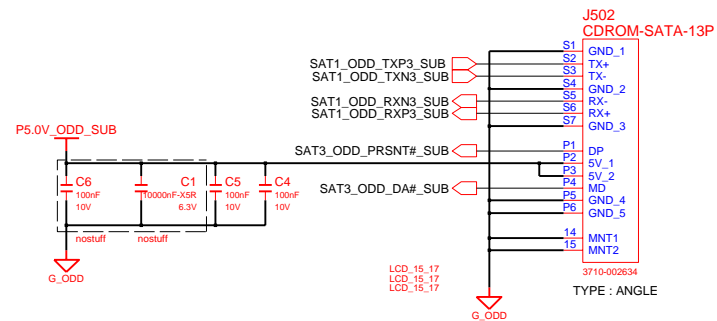


15.6" / 17.3"

MAIN TO SUB : SATA ODD CONN



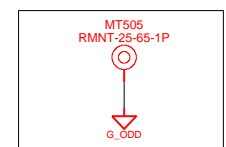
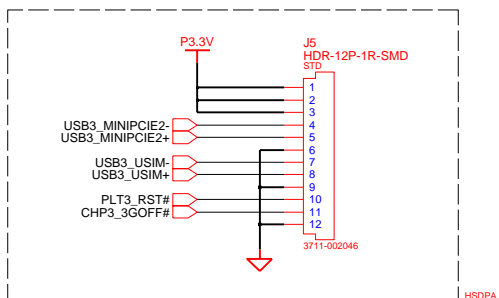
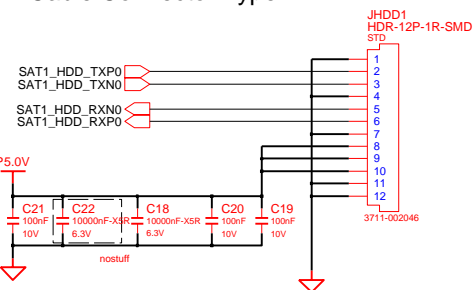
SATA ODD CONN



SATA HDD CONN

MAIN to HSDPA SUB

Cable Connector Type

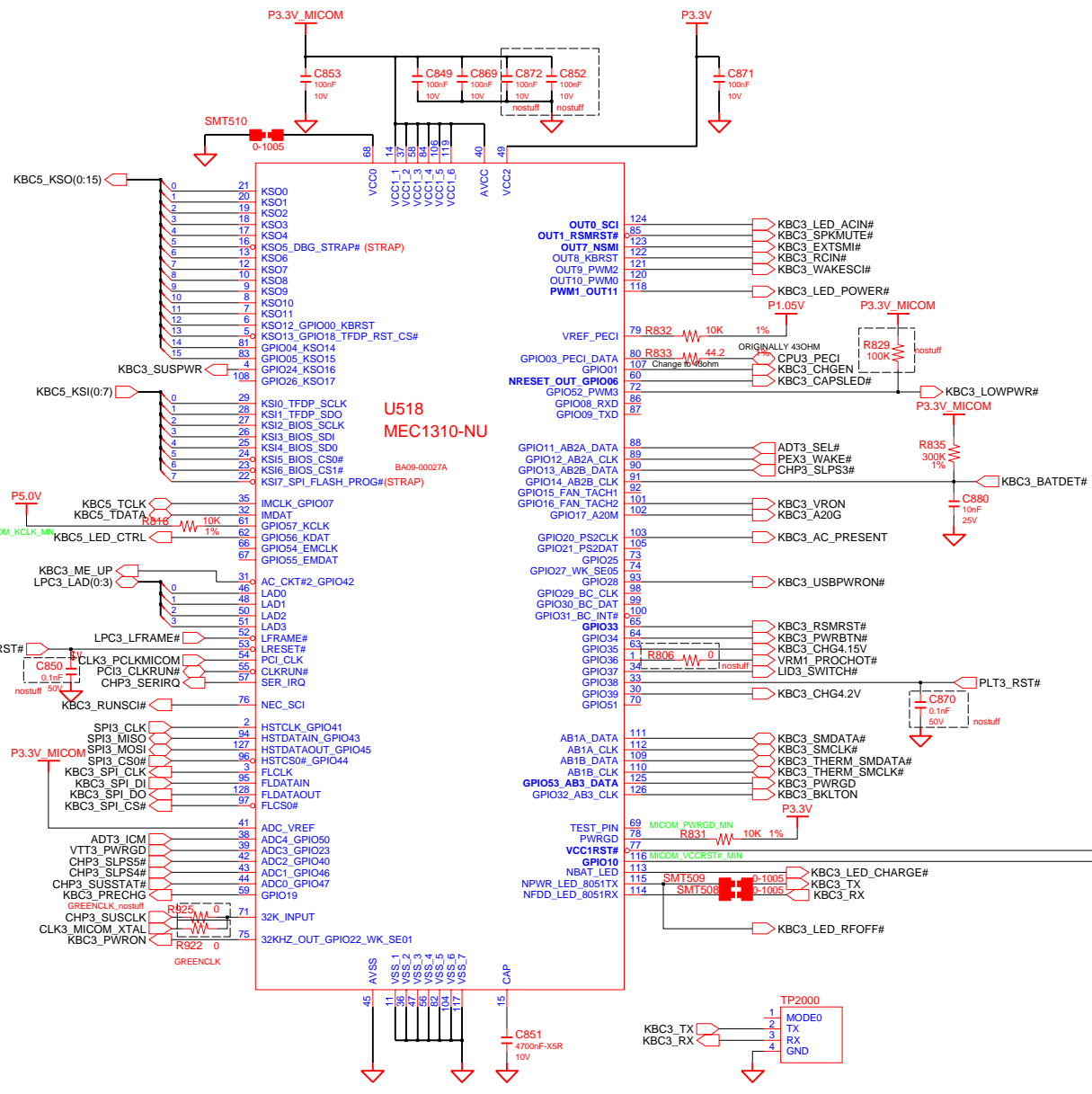


ODD sub board mount hole

DESIGN	Gu Hui	DATE	1/03/2011	TITLE	Scala2-R	SAMSUNG ELECTRONICS
CHECK	SJ Wu	DEV. STEP	ADV	SATA_DEVICES		
APPROVAL	BC LEE	REV	rev. 0.1	SATA I/F Conn		
MODULE CODE		LAST EDIT				
					January 20, 2011 18:59:20 PM	PAGE 32 OF 48

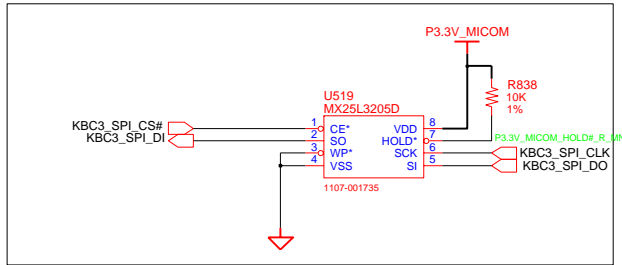
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MAIN BOARD (MICOM)

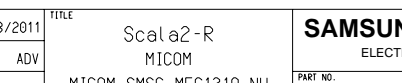
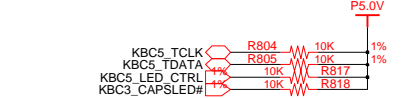
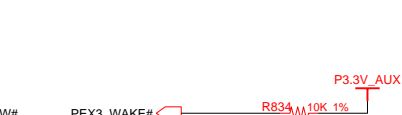
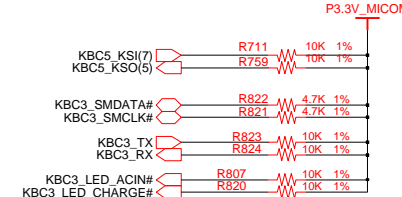
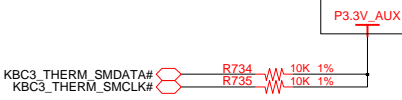


BE CAUTION SPI ROM SIZE!!

SPI_ROM_SOCKET



Connected to SML1 in PCH



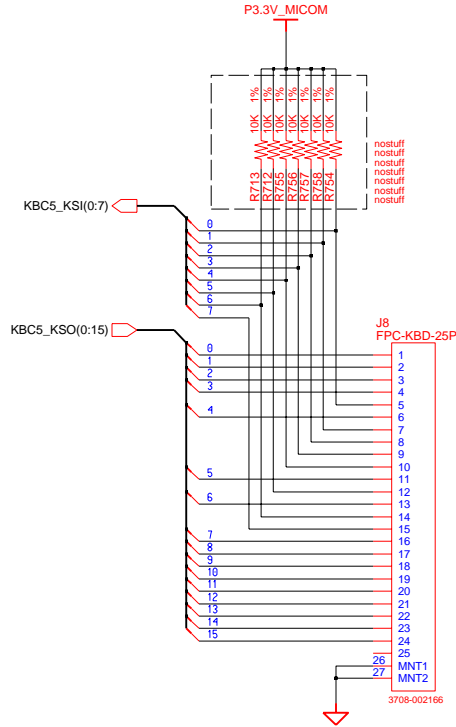
DRAW	Gu Hui	DATE	1/03/2011	TITLE	Scala2-R MICOM	SAMSUNG ELECTRONICS
CHECK	SJ Wu	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	rev. 0.1		MICOM_SMSC_MEC1310-NU	PART NO.
MODULE CODE		LAST EDIT	January 20, 2011 18:59:20 PM	PAGE	33	BA41-01XXXXA
					OF	48

3

Micom Glue Logic

2

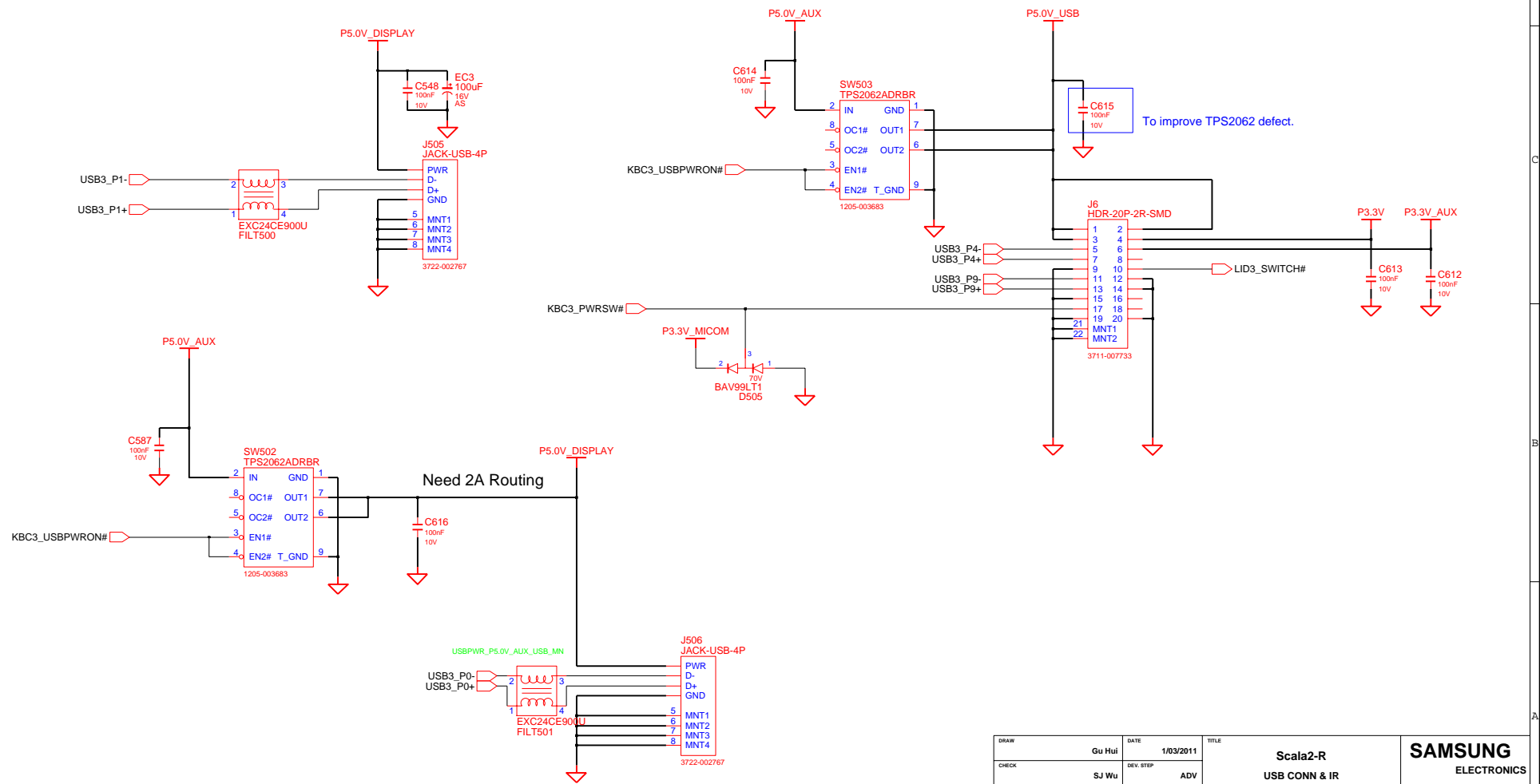
KEYBOARD



DRAW	Gu Hui	DATE	1/03/2011	TITLE	Scala2-R	SAMSUNG ELECTRONICS
CHECK	SJ Wu	DEV. STEP	ADV	MICOM GLUE LOGIC		
APPROVAL	BC LEE	REV	rev. 0.1	MICOM GLUE LOGIC	PART NO. BA41-01XXXA	
MODULE CODE	LAST EDIT				January 20, 2011 18:59:20 PM	PAGE 34 OF 48

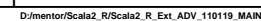
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POWER S/W SUB B'D CONNECTOR
MAIN to SUB

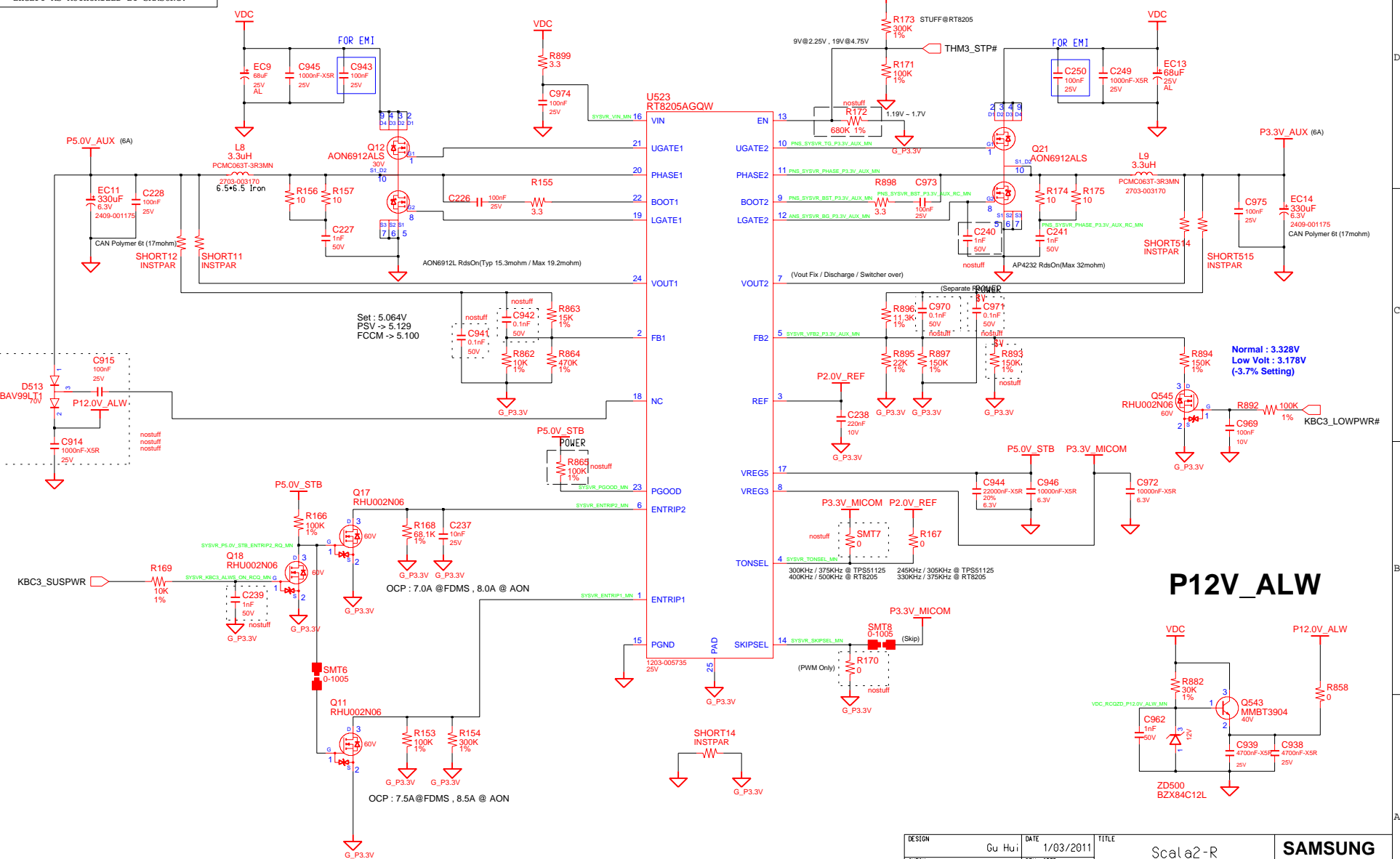


DRAW	Gu Hui	DATE	1/03/2011	TITLE	Scala2-R	SAMSUNG ELECTRONICS
CHECK	SJ Wu	DEV. STEP	ADV	USB CONN & IR		
APPROVAL	BC LEE	REV	rev. 0.1	USB & IR		
MODULE CODE		LAST EDIT				PART NO. BA41-01XXXA
					January 20, 2011 18:59:20 PM	PAGE 35 OF 48

CHARGER & POWER MANAGEMENT

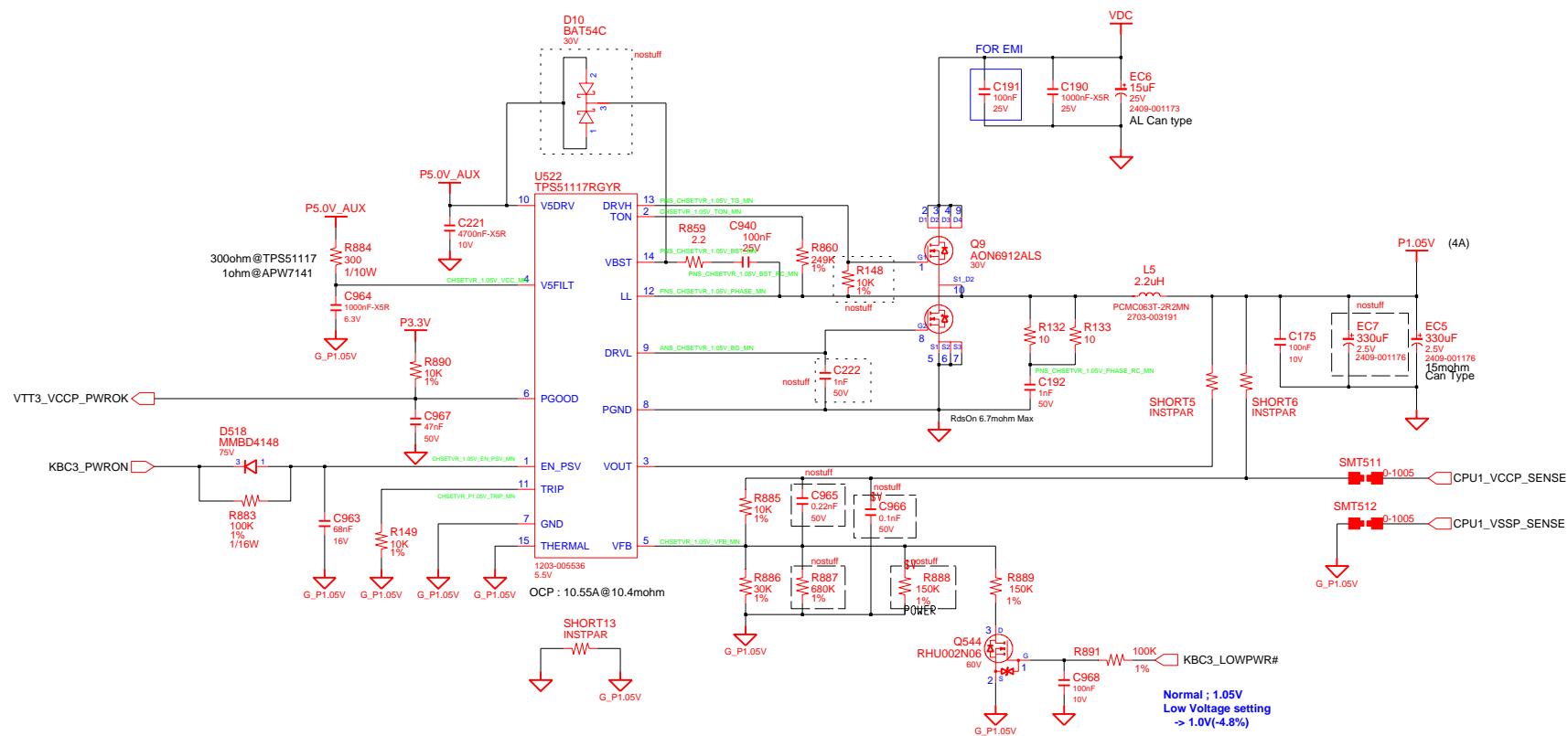



P3.3V_AUX & P5.0V_AUX



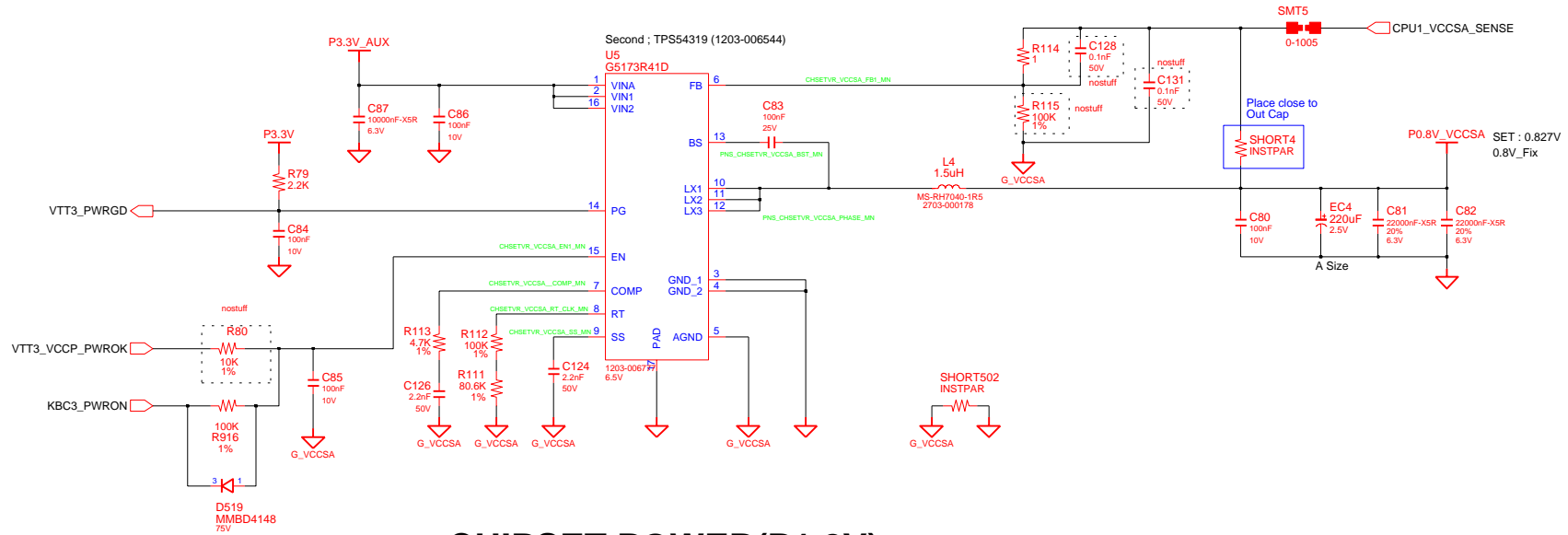
DESIGN	Gu Hui	DATE	1/03/2011	TITLE Scala2-R P3.3V_AUX / P5.0V_ALW P3.3V_AUX /P5.0V_AUX	SAMSUNG ELECTRONICS
CHECK	SJ Wu	DEV. STEP	ADV		
APPROVAL	BC LEE	REV	rev. 0.1		
MODULE CODE	LAST EDIT		January 20, 2011 18:59:20 PM		
					PART NO. BA11-01XXXX

CHIPSET POWER(P1.05V)

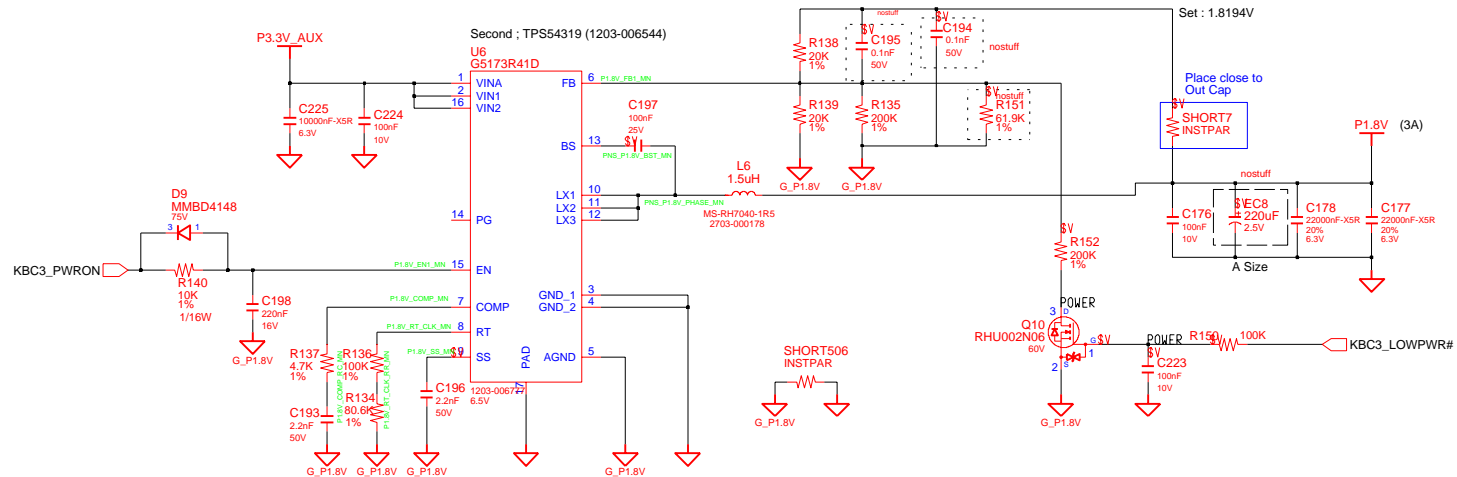


DRAW	Gu Hui	DATE	1/03/2011	TITLE			
CHECK	SJ Wu	DEV. STEP	ADV				
APPROVAL	BC LEE	REV	rev. 0.1	P1.05V(Chipset Power)		PART NO.	BA41-01XXXX
MODULE CODE	undefined	LAST EDIT		January 20, 2011 18:59:20 PM	PAGE	38	OF 48

CHIPSET POWER(VCCSA)

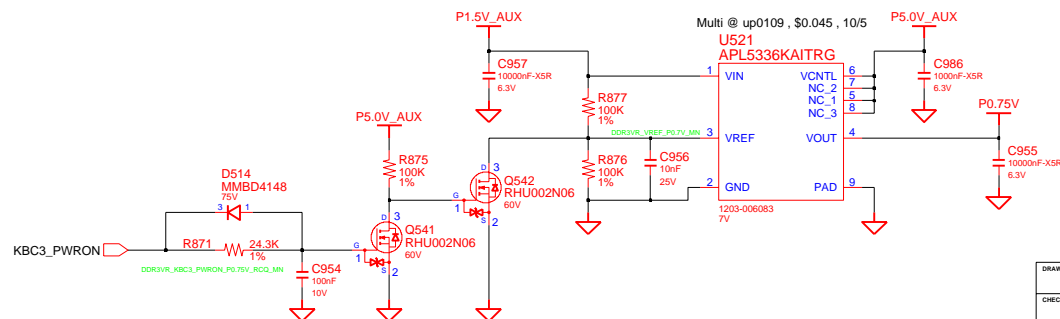


CHIPSET POWER(P1.8V)



DESIGN	Gu Hui	DATE	1/03/2011	TITLE	Scala2-R	SAMSUNG ELECTRONICS
CHECK	SJ Wu	DEV. STEP	ADV		P1.1V_VTT	
APPROVAL	BC LEE	REV	rev. 0.1		P0.8V(Chipset Power)	PART NO.
MODULE CODE		LAST EDIT	January 20, 2011 18:59:20 PM	PAGE	39	OF 48

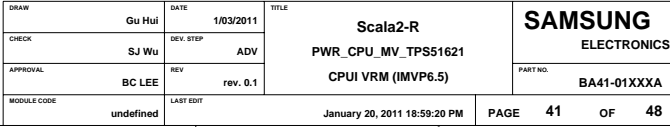
DDR3 VTT(0.75V)



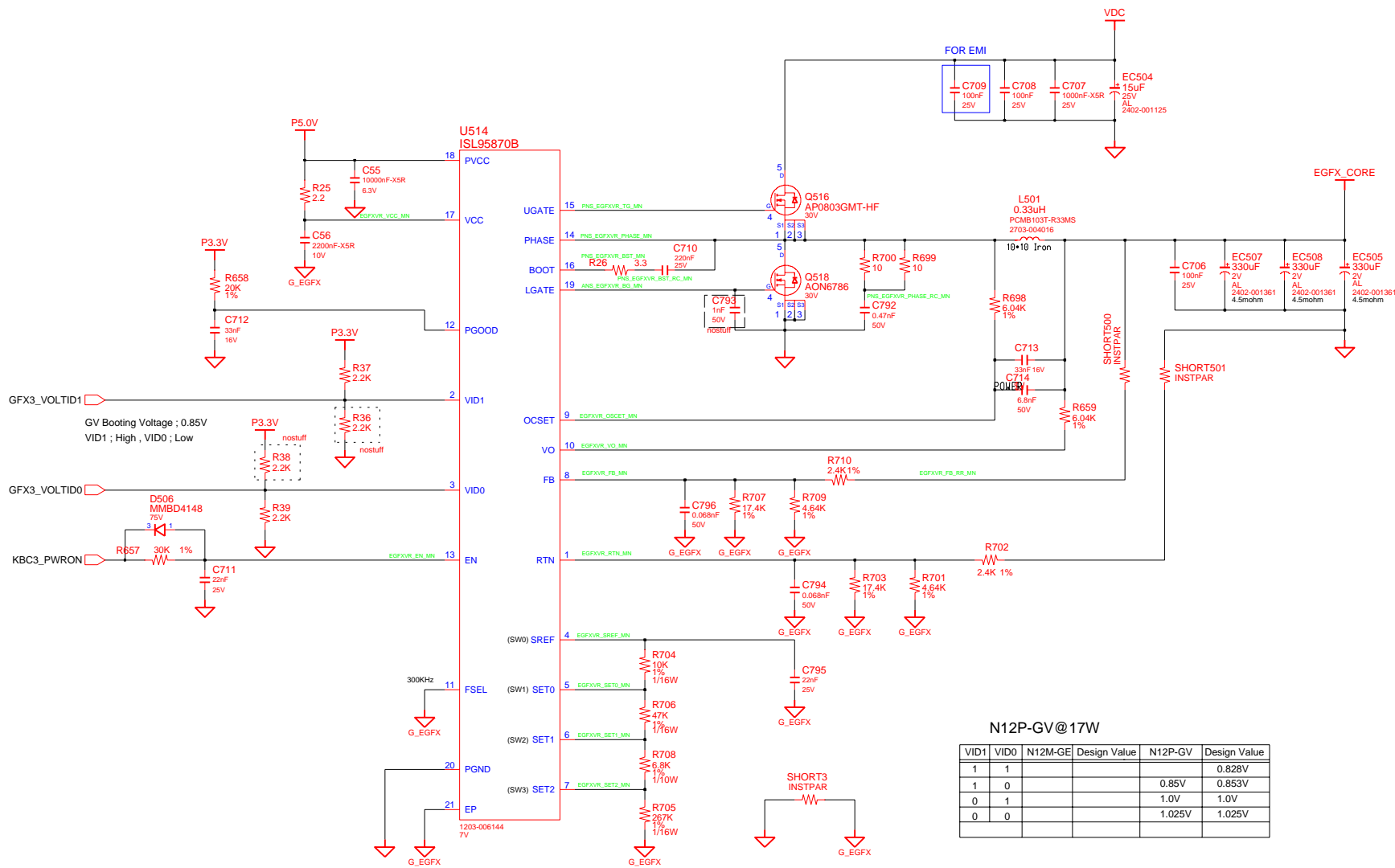
DRAW	Gu Hui	DATE	1/03/2011	Scala2-R PWR_MEMORY DDR3 POWER	SAMSUNG ELECTRONICS			
CHECK	SJ Wu	DEV. STEP	ADV					
APPROVAL	BC LEE	REV	rev. 0.1					
MODULE CODE	undefined	LAST EDIT						
				January 20, 2011 18:59:20 PM	PAGE	40	OF	48

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57K@283KHz



External GFX Core Power



N12P-GV@17W

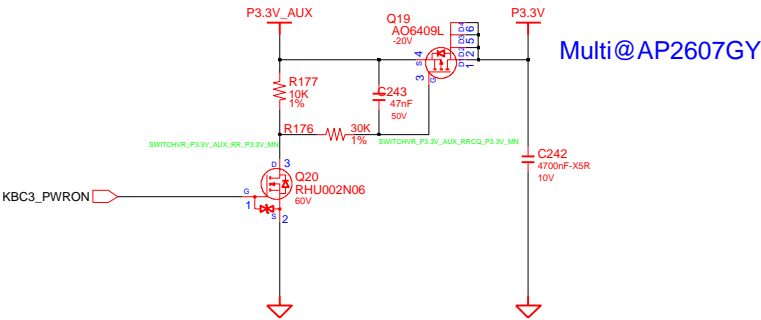
VID1	VID0	N12M-GE	Design Value	N12P-GV	Design Value
1	1				0.828V
1	0			0.85V	0.853V
0	1			1.0V	1.0V
0	0			1.025V	1.025V

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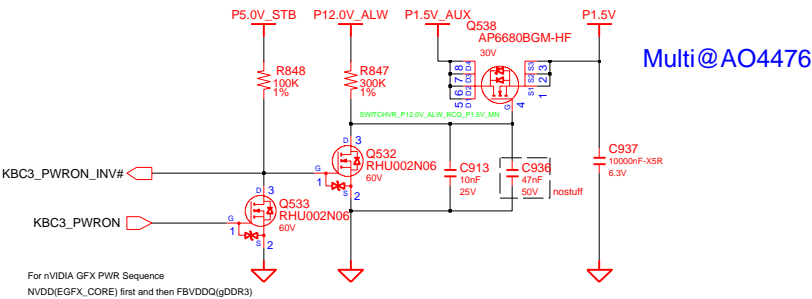
Switched Power

P5.0V -> P3.3V -> EGFX_CORE -> P1.8V ->P1.5V -> P0.75V -> P1.05V -> P0.8V_VCCSA -> CPU_CORE

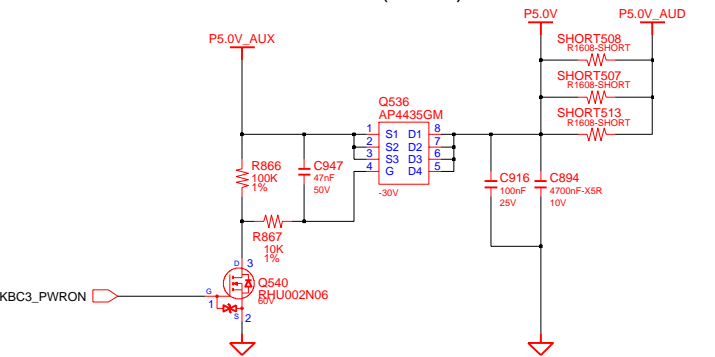
Switched Power On (P3.3V)



Switched Power On (P1.5V)



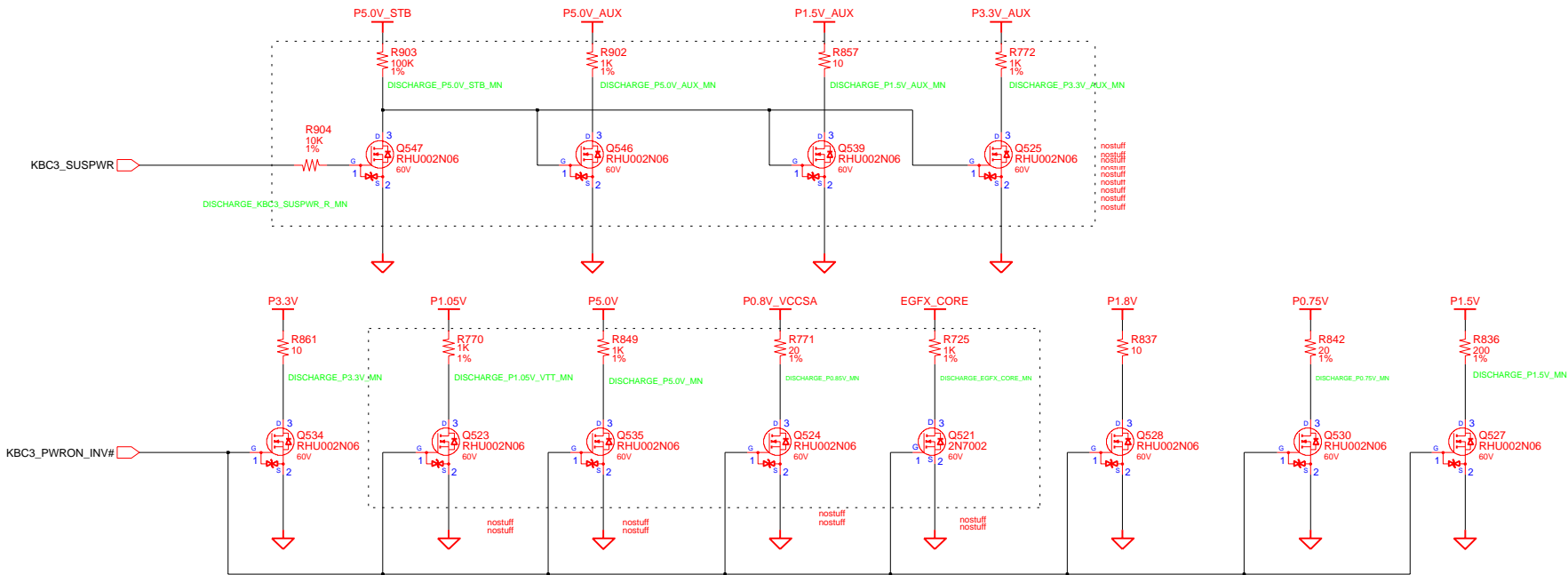
Switched Power On (P5.0V)



DRAW	Gu Hui	DATE	1/03/2011	TITLE	Scala2-R	SAMSUNG
CHECK	SJ Wu	DEV. STEP	ADV	PWR_MV_DISCHARGER	SWITCHED POWER	ELECTRONICS
APPROVAL	BC LEE	REV	rev. 0.1			PART NO.
MODULE CODE	undefined	LAST EDIT	January 20, 2011 18:59:20 PM			BA41-01XXXA
				PAGE	43	OF 48

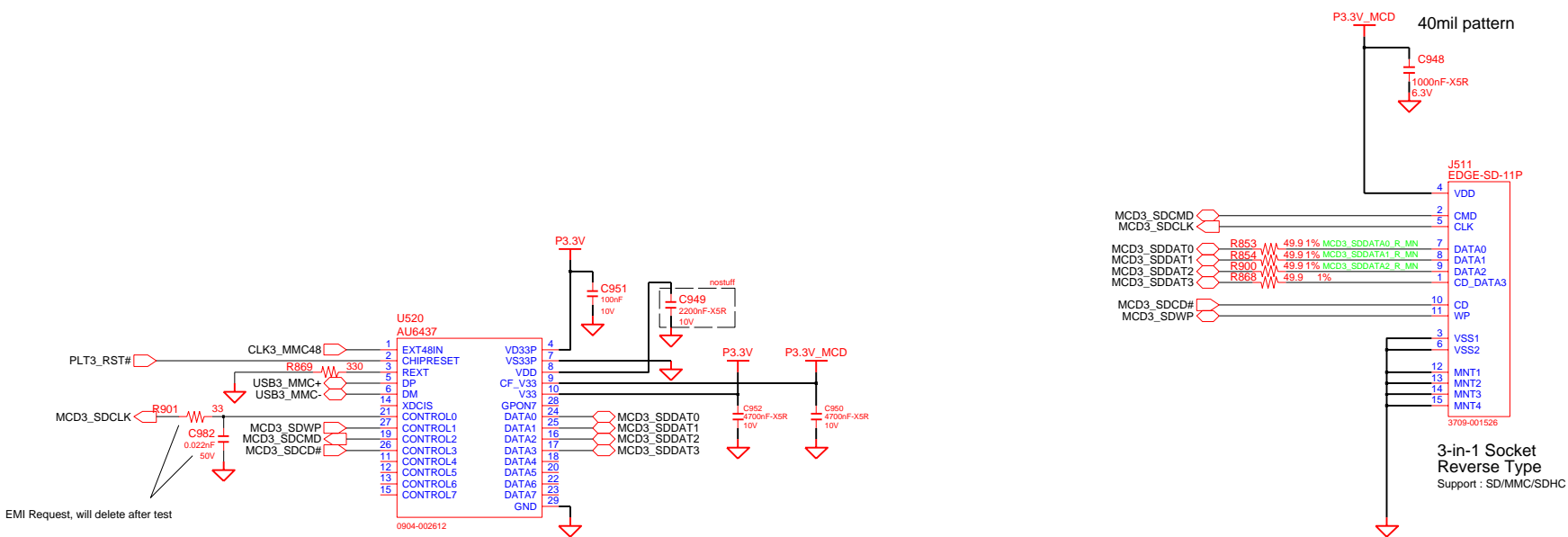
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POWER DISCHARGER



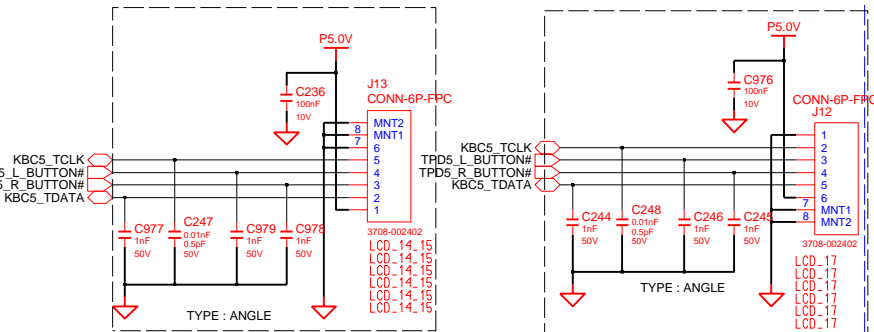
DESIGN	Gu Hui	DATE	1/03/2011	Scala2-R SUB BOARD1 Power Discharger		SAMSUNG ELECTRONICS	
CHECK	SJ Wu	DEV. STEP	ADV				
APPROVAL	BC LEE	REV	rev. 0.1				
				PART NO.		BA41-01XXXX	
MODULE CODE	LAST EDIT			January 20, 2011 18:59:20 PM		PAGE	45 OF 48

AU6437 (4-in-1)



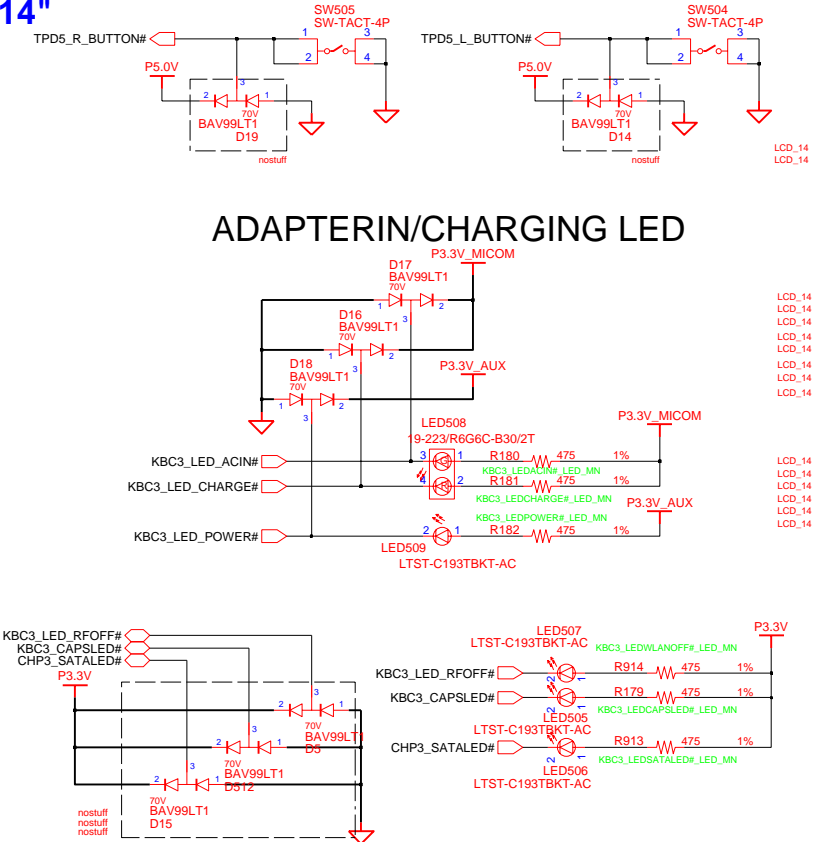
DESIGN	MS YANG	DATE	1/03/2011	TITLE	Jinmao-R	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	ADV	AU 6437	AU 6437	
APPROVAL	BL LEE	REV	rev. 0.3	AU 6437		
MODULE CODE		LAST EDIT	January 18, 2011 08:10:20 AM	PAGE	46 OF 48	

TOUCHPAD

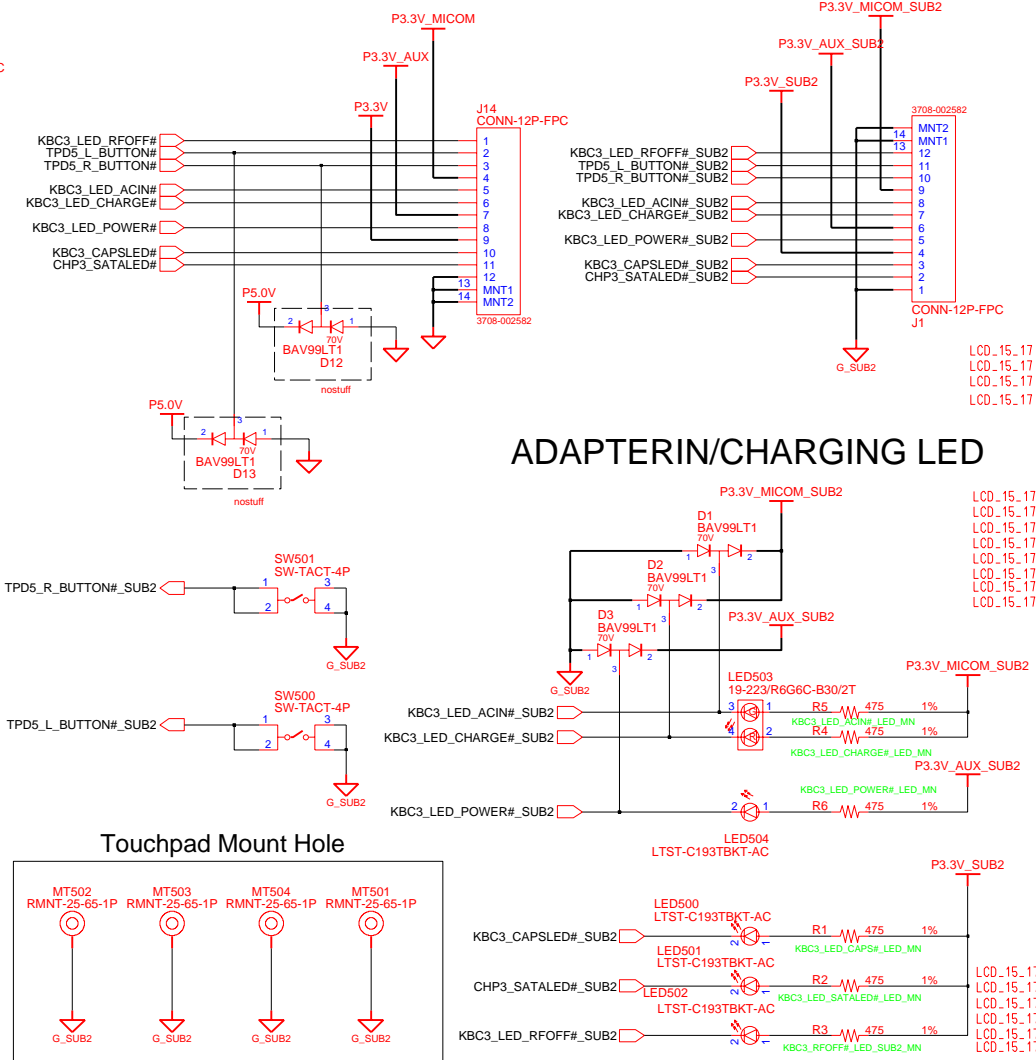


14"

ADAPTERIN/CHARGING LED

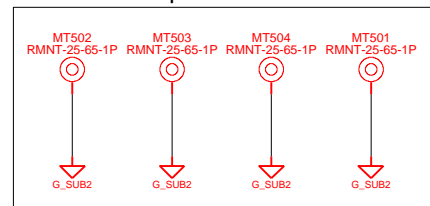


15.6" & 17.3" TOUCHPAD MAIN TO SUB TOUCHPAD SUB TO MAIN



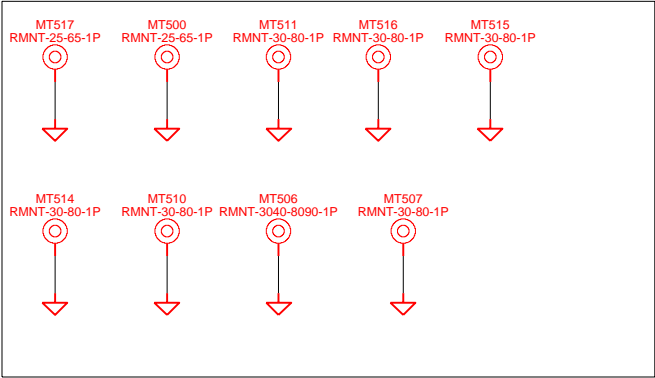
ADAPTERIN/CHARGING LED

Touchpad Mount Hole

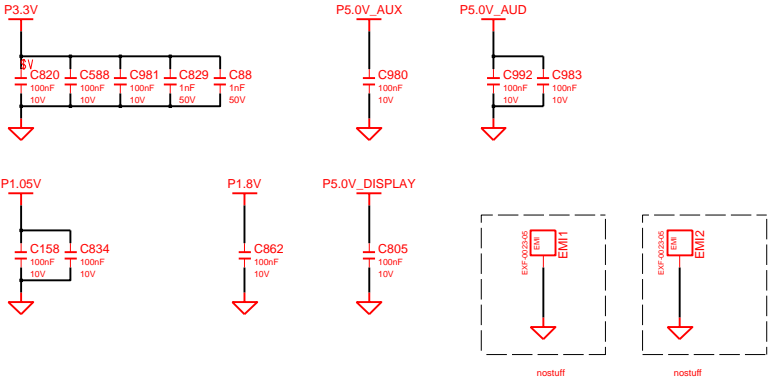
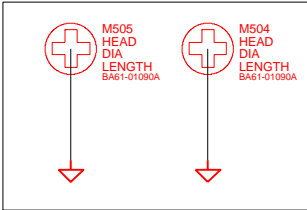


DRAW	MS YANG	DATE	1/03/2011	TITLE	Jinmao-R	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	ADV	Touchpad	Touchpad	
APPROVAL	BL LEE	REV	rev. 0.3			
MODULE CODE		LAST EDIT				
January 18, 2011 08:10:20 AM						PAGE 47 OF 48

Mainboard Mount ((25-65)X2EA, (30-80)X7EA)



PCH Thermal



DESIGN	MS YANG	DATE	1/03/2011	TITLE	Jinmao-R	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	ADV	MNT hole		
APPROVAL	BL LEE	REV	rev. 0.3	MNT hole	PART NO. BA41-01XXXA	
MODULE CODE	LAST EDIT				January 18, 2011 08:10:20 AM	PAGE 48 OF 48

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